An On-Chip ESD Protection Circuit with Low Trigger Voltage in BiCMOS Technology

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Abstract—A novel low-trigger dual-direction on-chip electrostatic discharge (ESD) protection circuit is designed to protect integrated circuits (ICs) against ESD surges in two opposite directions. The compact ESD protection circuit features low triggering voltage (∼7.5 V), short response time (0.18–0.4 ns), symmetric deep-snapback I–V characteristics, and low on-resistance (∼1Ω). It passed the 14-kV human body model (HBM) ESD test and is very area efficient (∼80 V/μm width). The new ESD protection design is particularly suitable for low-voltage or multiple-power-supply IC chips.

Index Terms—ESD protection, low trigger voltage.

I. INTRODUCTION

ELECTROSTATIC discharge (ESD) failure can be a major IC reliability problem, and on-chip ESD protection structures are used to protect IC chips against ESD damages [1]–[5]. ESD protection design becomes a challenging task particularly in high-speed very deep-submicron (VDSM) mixed-signal designs that call for fast response, multiple-trigger-voltage and area-efficient ESD protection solutions with ever higher ESD failure threshold voltage (ESDV) [6]. In principle, an ESD protection structure turns on during an ESD event and forms a current discharge path to shunt the huge ESD current as well as to clamp the voltage of I/O pads to a sufficiently low level to prevent ICs from being damaged [1]. The current shunting path comes from either an active device, offering an active path with desired low on-resistance, or a parasitic device, forming a passive path usually with relative higher on-resistance. A complete ESD protection solution [6] must protect each I/O pin against ESD surges in all stressing modes with respect to both power supply (VDD) and ground, e.g., positive-to-VDD (PD), negative-to-VDD (ND), positive-to-ground (PS), and negative-to-ground (NS), as well as from VDD to ground (DS). A typical ESD protection scheme is illustrated in Fig. 1(a) where usually an active discharging path forms in one direction only (i.e., ND and PS), with a parasitic current path functioning in the opposite direction (i.e., PD and NS). This parasitic discharging channel is usually the limiting factor during an ESD event. To alleviate such problems, a second stand-alone active ESD device may be used to replace the parasitic discharging channel. However, more silicon is consumed, which leads to more parasitic effects. In addition, multiple-power-supply mixed-signal ICs require optimized ESD protection structures with specially tailored triggering voltages. In this paper, a novel low-triggering dual-direction ESD protection circuit is reported that provides ESD protection in all stressing modes (ND, PD, NS, and PS), with a complete ESD protection scheme as illustrated in Fig. 1(b). This compact design delivers higher ESDV value while consuming less silicon, providing better ESD performance with less parasitic effect.

II. CIRCUIT DESCRIPTION

A. Dual-Direction ESD Protection Structure

The new low-trigger dual-direction ESD protection circuit consists of one core ESD device offering dual-direction ESD protection and a compact current-source type subcircuit providing low-trigger voltage. The core device, with its BiCMOS implementation, illustrated in Fig. 2(a), is a symmetrical two-terminal NPNPN structure comprising one lateral PNP transistor (Q1 = P2N3P1), two vertical NPN transistors (Q2 = N1P2N3 and Q3 = N2N4P3), and four parasitic resistors R1, R2, R3, and R4. The structure is internally connected to a two-terminal device (denoted as A and K) in such a way that, functionally, it forms a pair of reverse interconnected thyristors (upper one: Q1, Q2, R1, and R3, and lower one: Q1, Q3, R2, and R4) with its equivalent circuit illustrated in Fig. 2(b). Under normal IC operating condition, the device is off. During an ESD event, it is triggered to form current shunt paths in both directions to drain the surge current.
Fig. 2. (a) A sample cross-section of the new ESD protection structure implemented in a BiCMOS technology with a deep $N^+$ isolation layer designed for noise isolation. The two terminals are connected to the I/O pin and ground (or $V_{SS}$), as shown in Fig. 1. It forms two thyristors ($Q_1$, $Q_3$, $R_2$ and $R_4$, and $Q_1$, $Q_2$, $R_1$ and $R_3$) to discharge ESD surges in both directions. Its triggering voltage is controlled by either junction breakdown, which is normally too high for sub-5-V applications. (b) Circuit schematics for the new ESD protection structure show a pair of thyristors ($Q_1$, $Q_3$, $R_2$ and $R_4$, and $Q_1$, $Q_2$, $R_1$ and $R_3$) serving as ESD discharging units in the two opposite directions.

as well as to clamp the I/O pad voltage to a sufficient low level. When a positive ESD pulse is applied to terminal $A$ with respect to terminal $K$ (e.g., ND or PS case in Fig. 1(b), the BC junction ($N_3P_3$) of $Q_2$ is reverse biased to reach its reverse breakdown. The generated holes are mainly collected by the negative terminal $K$ through the $N_3P_3(P^+)$ layer. Since both the $P_3(P^+)$ and $N_3(N^+)$ layers are connected to $K$, $V_{BEE} (P_3N_3)$ of $Q_3$ increases and eventually turns on $Q_3$. The lower thyristor ($P_3N_3P_2N_2$) is therefore triggered off and driven into deep snapback region with very low holding voltage $V_{th} (\leq 2 \text{ V})$ and on-resistance $R_{on}$. An active discharging path with negligible impedance is therefore formed to shunt the huge current surge in the direction of $A$ to $K$. The very low holding voltage $V_{th}$ serves to clamp the I/O pad voltage to a sufficient low level ($\leq 2 \text{ V}$). The device thus protects an IC chip against ESD stresses in one direction ($A$ to $K$). Similarly, if a negative ESD pulse appears at terminal $A$ with respect to terminal $K$ (alternatively saying, a positive ESD pulse from terminal $K$ to $A$, e.g., PD or NS case as in Fig. 1(b), the upper thyristor ($P_3N_3P_2N_2$) follows the same principle to protect against the ESD stress in the opposite direction (from $K$ to $A$). Therefore, one single such device provides dual-direction ESD protection. It is worth noting that the critical trigger voltage ($V_{th} \approx 23 \text{ V}$ in this design) of this new structure is determined by the BC-junction breakdown voltage of the PNP transistor, $Q_2$, which is fixed for the given BC-junction layers. However, in multiple-$V_{DD}$ designs, flexible $V_{th}$ values are preferred for optimal ESD performance. A layer engineering technique, in which proper layers are selected for the $Q_2$, may be used to adjust the $V_{th}$ values in BiCMOS technologies. A more efficient solution to varying $V_{th}$ is to use a trigger-assist subcircuit to realize a low trigger voltage $V_{th}$, which is highly desired in sub-5-V applications.

B. Low-Trigger ESD Protection Circuit

The principle of the low-trigger ESD circuit is that an external current source is used to assist the triggering of the core ESD protection structure described in Section II-A. Fig. 3 shows the low-trigger dual-direction ESD protection circuits consisting of the core dual-direction ESD protection device and a low-trigger subcircuit. The core ESD device is used in a four-terminal format (terminals, (1), (2), (3), and (4)) in this circuitry as compared to the two-terminal mode as in the stand-alone ESD device described in Fig. 2. The two extra terminals, (5) and (6), serve as input ports for injection of external...
Fig. 4. Sample $I-V$ characteristics of the new core ESD structure. (a) $I-V$ from static ESD simulation shows symmetric operation, deep-snapback, active discharging paths in both directions, triggering point and holding point that are critical in ESD design. Relatively high trigger voltage is observed. (b) $I-V$ curve of a 100-$\mu$m-wide new ESD protection structure measured using a Tektronix Curve Tracer shows symmetric and deep-snapback operation as predicted by ESD simulation. (c) $I-V$ characteristic curve of a 100-$\mu$m-wide new ESD protection structure measured (Y-axis, current versus voltage, lower X-axis) using a TLP tester in A-to-K direction (Barth Electronics Model 4200) shows similar symmetric and deep-snapback operation. Instantaneous leakage current measured after each stress (upper X-axis, leakage versus voltage, lower X-axis) indicates negligible influence on IC chips under normal operation. The thermal breakdown threshold point coincides with the breaking point of the leakage that correlates to the ESDV level.

Current to assist triggering action. The low-trigger subcircuit comprises two pairs of identical Zener diodes, $D_1, D_2, D_3$, and $D_4$, connected back-to-back, and two resistors, $R_5$ and $R_6$. The low triggering voltage comes from the selected low breakdown voltage of the Zener diode that is around 7 V in this design. The whole ESD circuitry still operates as a two-terminal device (also denoted as $A$ and $K$), which conducts the same way as in the stand-alone core ESD device. Functionally, the new ESD circuitry consists of four possible current discharging paths, path 1 of $Q_1$ and $Q_2$ ($A$ to $K$), path 2 of $Q_1$ and $Q_2$ ($K$ to $A$), path 3 of $D_1$, $D_2$, and $R_5$ ($A$ to $K$), and path 4 of $D_3$, $D_4$, and $R_6$ ($K$ to $A$). Zener diodes, $D_1$ and $D_4$, are the current-source elements serving to provide external current for the core ESD device to trigger off at a considerably lower threshold voltage.
TABLE I

<table>
<thead>
<tr>
<th></th>
<th>Stand-alone Core ESD structure</th>
<th>Low-Trigger Voltage ESD Circuit</th>
<th>Zener Diode</th>
<th>ESD Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulation (V)</td>
<td>Test (V)</td>
<td>Simulation (V)</td>
<td>Test (V)</td>
</tr>
<tr>
<td>( V_{th} )</td>
<td>23.32</td>
<td>23.85</td>
<td>6.55</td>
<td>-</td>
</tr>
<tr>
<td>( V_Z )</td>
<td>1.58</td>
<td>-1.6</td>
<td>-3</td>
<td>-1.6</td>
</tr>
<tr>
<td>( t_t ) (ns)</td>
<td>~0.18</td>
<td>-</td>
<td>0.4</td>
<td>-</td>
</tr>
<tr>
<td>( R_{on} ) (Ω)</td>
<td>0.74</td>
<td>0.6</td>
<td>0.55</td>
<td>2Ω</td>
</tr>
<tr>
<td>( ESDV )</td>
<td>8/100μm</td>
<td>8/100μm</td>
<td>8/100μm</td>
<td>8/100μm</td>
</tr>
<tr>
<td>( (KV)</td>
<td>16/100μm</td>
<td>*14/100μm</td>
<td>16/100μm</td>
<td>*14/100μm</td>
</tr>
</tbody>
</table>
* The upper limit of the ESD zener used is 14KV for HBM model test.

under positive (from \( A \) to \( K \)) and negative (from \( K \) to \( A \)) ESD pulses in two opposite directions, respectively. Diodes \( D_2 \) and \( D_3 \) serve to block current paths 3 and 4 from being directly opened due to forward turn-on of diodes \( D_1 \) or \( D_4 \) under positive ESD surge and negative ESD surge, correspondingly. In operation, during a positive ESD pulse (from \( A \) to \( K \), e.g., ND or PS mode) event, both the core ESD device and Zener diode \( D_3 \) are stressed by the ESD surge. Because \( D_1 \) is designed to have a low breakdown voltage, it will be reverse broken-down first and opens up the current path 3. As the voltage-drop across \( R_6 \) reaches to about 0.7 V, the BE junction of \( Q_3 (P_2N_5, V_{BE} \approx 0.7 \text{ V}) \) of the core ESD device becomes forward-on, which, in turn, turns on the core ESD device (from terminal \( A \) to \( K \), path 1 opens), as in the stand-alone core ESD device case. The whole ESD circuitry is therefore turned on at a much lower voltage \( (V_{th} = BV_{Zener} \approx 7.5 \text{ V}) \), instead of at \( \sim 23 \text{ V} \) as in the stand-alone core ESD device situation, and the low-impedance thyristor channel takes most of the ESD current. Path 4 is blocked because the voltage drop over \( R_6 \) effectively slows down the potential build-up over \( D_3 \) in the transient procedure. Similarly, in a negative ESD pulse event (from \( K \) to \( A \), e.g., PD or NS mode), \( D_4 \) breaks down at 8 V and opens path 4. The voltage build-up of \( R_6 \) will turn on the BE junction of \( Q_2 (P_1N_1) \), then triggers off the core ESD device (from terminal \( K \) to \( A \), path 2 opens). Therefore, this new ESD protection circuitry offers the desired low trigger voltage and provides ESD protection in two directions. Based upon this operating principle, one may choose a different external current source to enhance triggering of the core ESD device for low-voltage designs. It is therefore possible to adjust the triggering point to obtain suitable high-performance dual-polarity ESD protection unit for low-voltage or multiple-power-supply designs.

III. SIMULATION, MEASUREMENT, AND DISCUSSION

A new TCAD-based mixed-mode simulation approach was used in this design to predict ESD performance [7]. The ESD simulation method includes both electrothermal coupling and device-circuit coupling, which is a critical feature in ESD CAD design. An example simulated \( I-V \) characteristic for the core ESD protection structure is shown in Fig. 4(a), where the symmetric operation, deep-snapback, and low-impedance features are clearly observed, indicating that the design provides active current discharging paths in both directions. The triggering threshold \( V_{th} \) and holding point \( V_{th} \) data can be extracted directly. The low holding voltage ensures the desired low bond-pad voltage clamping. The extremely low on-resistance of \( \sim 1 \text{ Ω} \) in the deep snapback region provides very high current-handling capability, hence high ESDV level.

The design was implemented in a commercial 0.6-μm BiCMOS technology. The measured \( I-V \) characteristics using both quasi-static curve tracing and transient transmission-line-pulsing (TLP) techniques [8] are shown in Fig. 4(b) and (c) for the same core ESD device. The simulation and measurements match each other reasonably well, with typical parameters of \( V_{th} \sim 23 \text{ V}, V_{th} \sim 1.6 \text{ V} \) and \( R_{on} \sim 1 \text{ Ω} \), as summarized in Table I. The TLP measurements also include instantaneous leakage tests after each stressing step. The
The example $I-V$ curve of the complete low-trigger ESD protection circuit from transient simulation is shown in Fig. 5(a), where a reduced $V_{\text{th}}$ of $\sim 9$ V is readily observed. This reduced $V_{\text{th}}$ is controlled by the Zener diode $D_1$ (same for $D_4$ in the opposite direction) breakdown of around 6.55 V as indicated in its simulated $I-V$ characteristic shown in Fig. 5(b). Fig. 6 shows typical measured $I-V$ curves using a curve tracer in which low-trigger symmetrical $I-V$ characteristics are observed, as predicted by simulation. However, because of the integrated layout, no measurements can be conducted for the Zener diodes. The noticeable discrepancy between the $V_{\text{th}}$ and Zener breakdown voltage may be attributed to the voltage drops across $D_3$ and $R_3$ and possible accumulation time needed for potential building-up in transient operation. It is worth noting that the Zener diode can be replaced by many other types of current sources to reduce the trigger voltage.

Measurement also includes standard ESD zapping tests to evaluate final ESD performance level represented by the ESDV values. ESD zapping tests (using IMCS 1000 ESD Zapping Machine) showed that a 50-$\mu$m-wide device passed 4-kV human body model (HBM) zapping [9] (failed at 5 kV) and a 200-$\mu$m-wide part passed HBM 14 kV (upper limit of the tester used) without being damaged. This translates into a very high ESDV-to-Si ratio of about 80 V/$\mu$m width, which indicates the new design is extremely area-efficient ESD. A high ESDV-to-Si ratio means that a relative small size ESD circuit is needed to achieve the same or even higher ESDV specification that, in turn, will have less parasitic impact on the core IC chip—a highly desired feature for VDSM and RF IC designs. The measurement data are summarized in Table I.

The ESD simulation method also provides other valuable design insights. Fig. 7 shows a typical $V-t$ curve from which the triggering time ($t_1$) of the ESD circuitry is extracted. The observed very short $t_1$ ($\sim 0.18$ ns for the core ESD device and $\sim 0.4$ ns for the low-trigger ESD circuit) indicates that the new ESD circuit can respond to ESD pulses very fast, which is critical to successful ESD protection in high-speed applications. During ESD simulation, maximum lattice temperature ($T_{\text{max}}$) across the ESD structure is extracted instantaneously to investigate its thermal behaviors. Fig. 8 illustrates a typical internal $T_{\text{max}}$ distribution under ESD stressing in which the hot spot (i.e., potential thermal defect) can be located. A hot spot located deep in silicon as observed in this new structure indicates better heat dissipation capability, therefore higher ESD performance as confirmed by the measurements. The above comparison discussion also suggests that ESD simulation plays a substantial role in successful ESD protection designs.

**IV. CONCLUSION**

A successful design of a novel low-trigger dual-polarity ESD protection circuit is reported. The new ESD protection circuitry demonstrates low-trigger threshold ($V_{\text{th}} \sim 7.5$ V) that is suitable for low-voltage IC designs, symmetric deep-snapback ($V_{\text{th}} < 2$ V) $I-V$ characteristics, low on-resistance ($R_{\text{on}} \sim \Omega$), and fast response to ESD pulses ($t_1 < $ ns). The new design passes HBM 14-kV stressing, representing a high ESDV-to-Si ratio of $\sim 80$ V/$\mu$m width, and provides ESD protection in two opposite directions. This new ESD protection solution is particularly suitable for low-voltage or multiple-power-supply VDSM and RFIC applications. It also demonstrates that ESD simulation is valuable in practical ESD protection design.
REFERENCES


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