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Taurus-Topography

Topography Modeling for IC Technology

Taurus-Topography simulates topography modification processes such as deposition, etch, spi glass, reflow and chemical-mechanical polishing, in 2D or 3D cross-sections of arbitrarily shape semiconductor devices composed of multiple layers. One of Taurus-Topography's most import features is the physically based topography models for accurate characterization of deposition a etch of different materials. Taurus-Topography, capable of multiprocess simulation, lets you tac issues ranging from the most complex three-dimensional local interconnect problems in DRAM technology to reliability issues associated with void formation during deposition.

TAURUS-TOPOGRAPHY HELPS YOU:

- Create accurate three-dimensional interconnect structures.
- Create cross-sectional structures resulting from multiple processes of state-of-the-art technology.
- Study all topography-related process integration issues.
- Simulate profile evolutions of deposition/etching processes, including APCVD, LPCVD, PECVD, HDP CVD, PVD, wet etch, reactive ion etch, sputter etch, high-density plasma e and many other semiconductor manufacturing processes.
- Study void formation mechanisms and provide guidelines for solutions.
- Simulate etch back planarization.
- Study reactive ion etch (RIE) lag effect.
- Characterize high aspect ratio trenching.
- Emulate local CMP effects at micro-structure scale.
- Emulate reflow process.
- Model shrinkage of spin on glass (SOG).
- Characterize plasma discharge and sheath transport mechanisms.
- Characterize plasma velocity and energy distribution at wafer surface.

VOID FORMATION DURING PLASMA-ENHANCED CVD

Inter-level dielectric processes often create voids. The understanding of the position, size and characteristics of these voids and their dependency on process and initial topographic conditior critical for the incorporation of a deposition process in a submicron multi-layer integration projec Taurus-Topography can be used to study the dependency of voids' shapes and position for any of layout variations. Comparison of the experimental result (Figure 1a) with the simulated result (Figure 1b) shows the excellent agreement obtained when simulating an oxide PECVD depositi process. The increase in opening width creates smaller and more superficial voids than narrow openings.

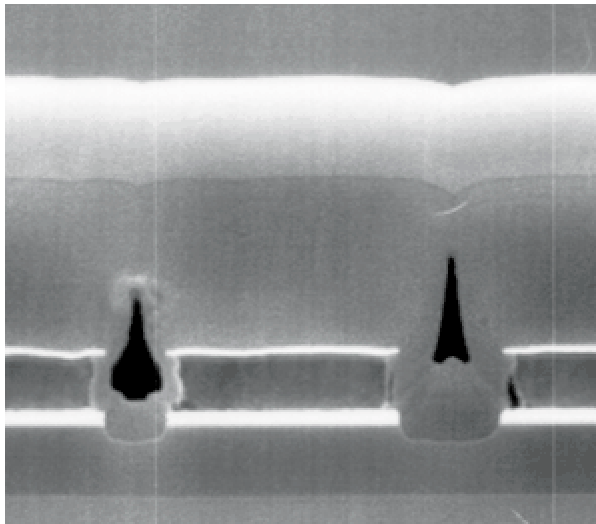


Figure 1a: Experimental Result

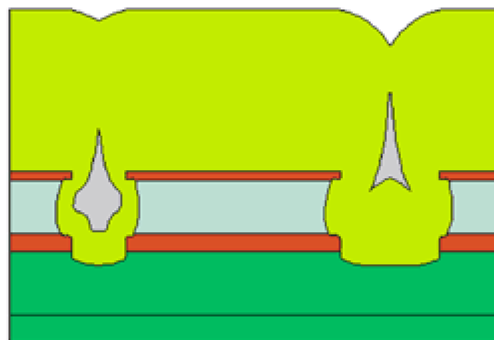


Figure 1b: Simulation of void formation

TAURUS-TOPOGRAPHY SIMULATION OF TRENCH ISOLATION

Trench isolation technology is commonly used for high-performance complementary bipolar devices. For process design purposes it is necessary to run topography simulation to model crit geometry features, including trench bottom rounding, void formation during trench filling, side w and bottom coverage, and the shape of polysilicon spacers. Figure 2a shows the experimental picture of a typical trench isolation structure. Simulation was done by applying an integration of Taurus-Topography's PECVD, LPCVD, anisotropic etch and conformal deposition modules. Th simulation result is shown in Figure 2b. All the key features are well captured.

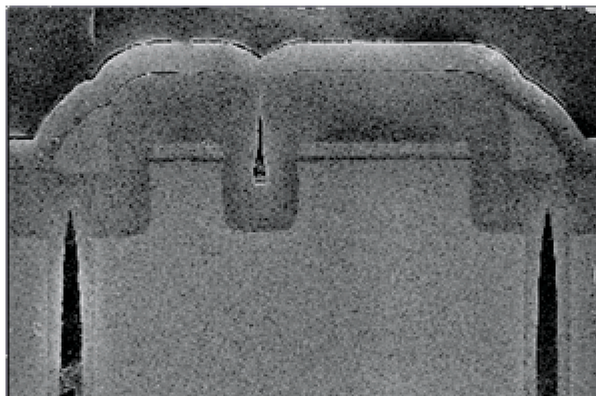


Figure 2a: Experimental example of trench isolation

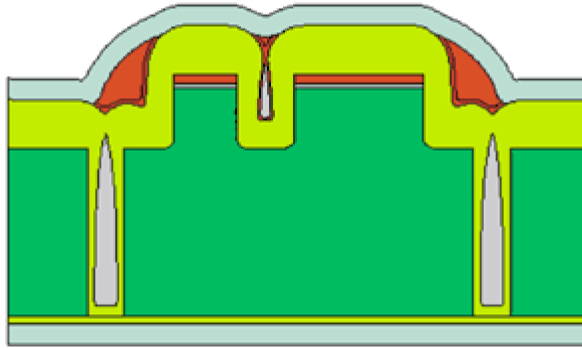
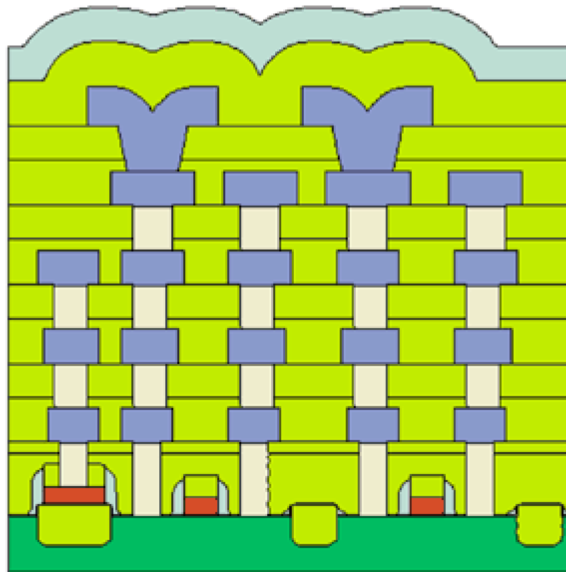


Figure 2b: Simulation of trench isolation

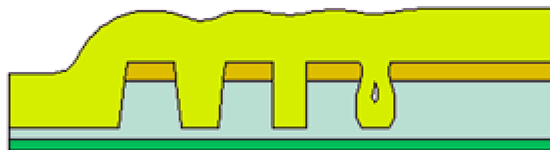
TOPOGRAPHY SIMULATIONS IN TAURUS-TOPOGRAPHY

SIMULATION METHODOLOGY:

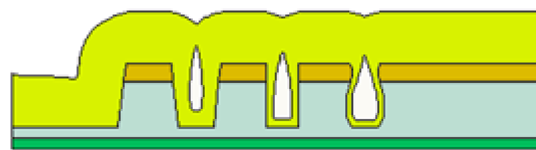
Step 1: Quick integration to build a multi-layer structure.
Step 2: Accurate, isolated unit process simulation.



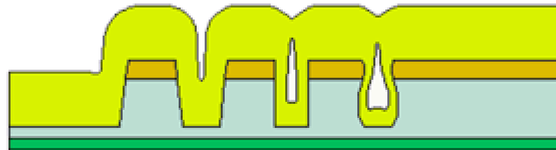
Process integration



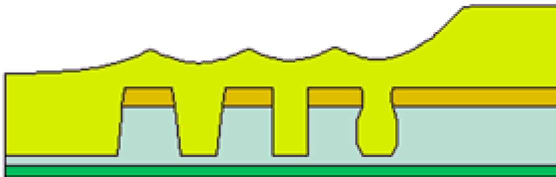
APCVD



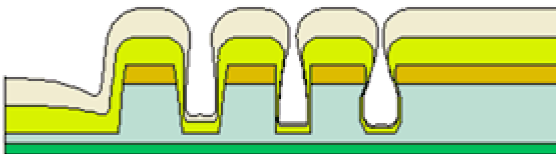
LPCVD



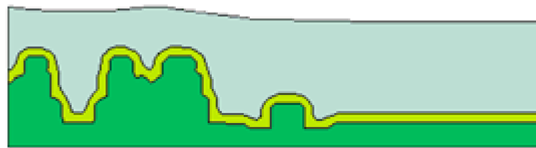
PECVD



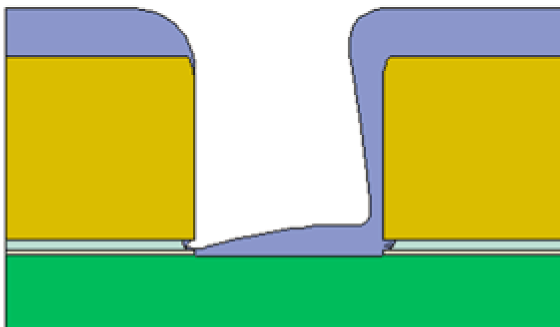
HDP CVD,



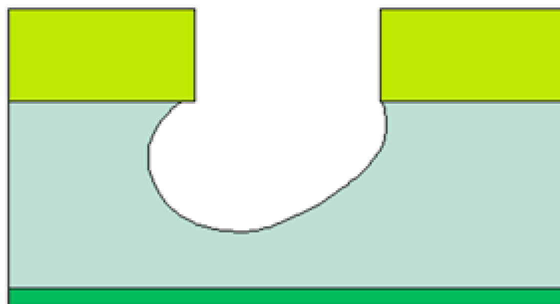
PVD for metalization



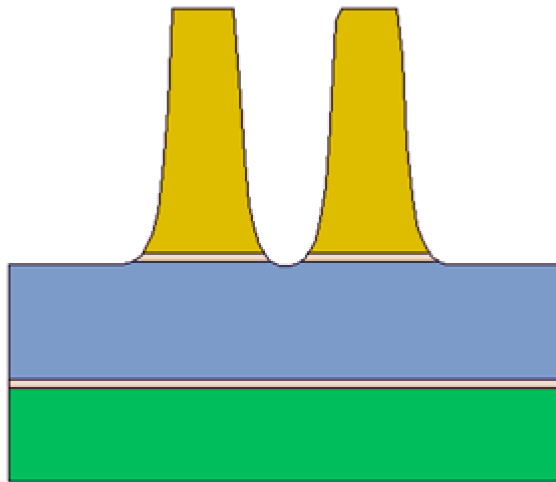
Spin Deposition

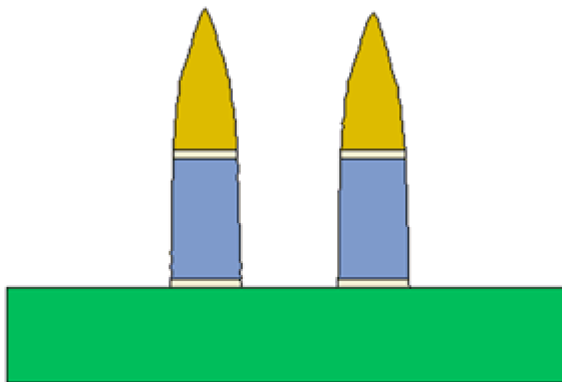


Hemispherical deposition

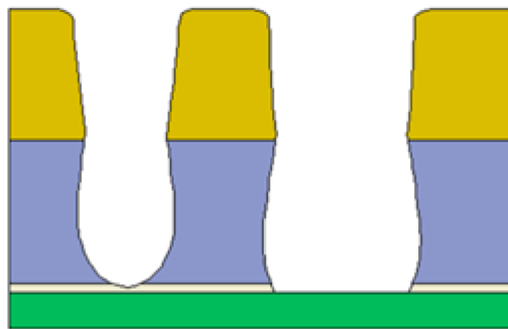


Hemispherical etch

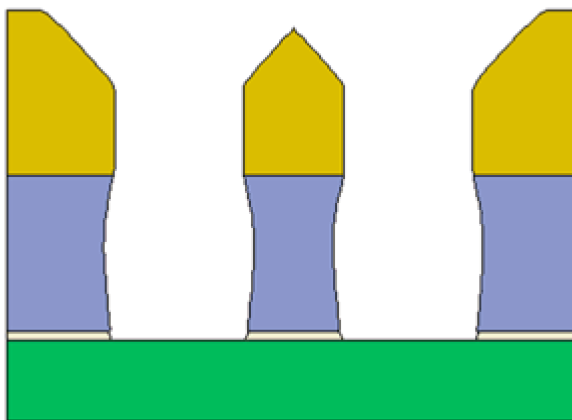




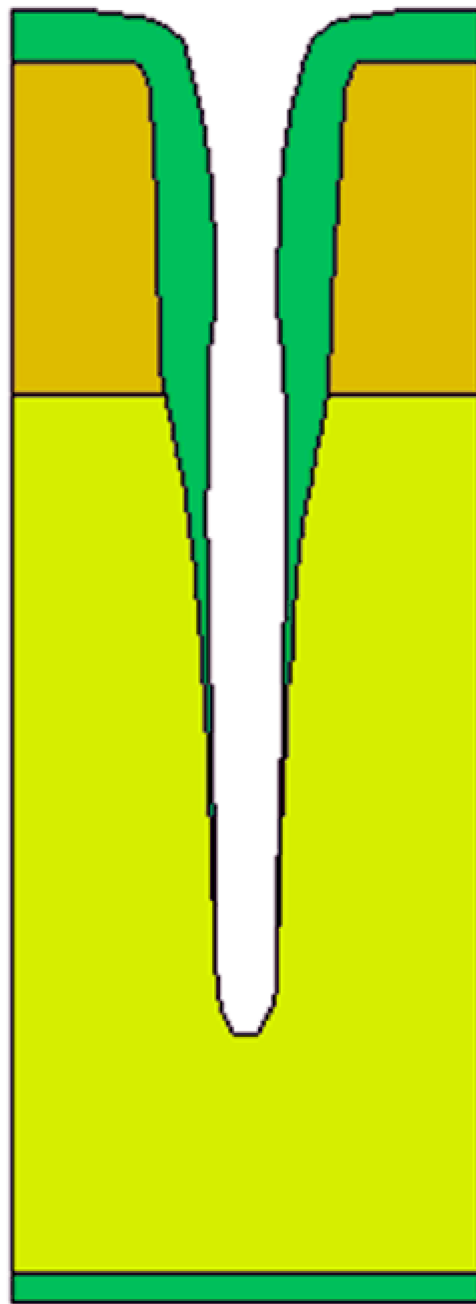
Ion milling

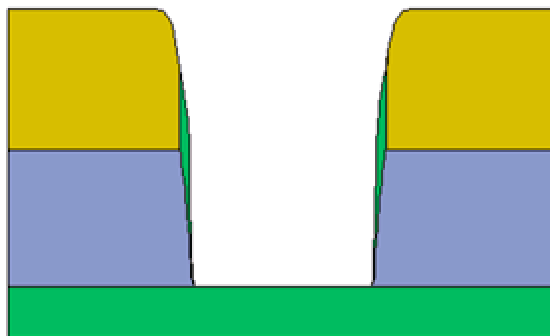


Reaction ion etch (showing lag effect).

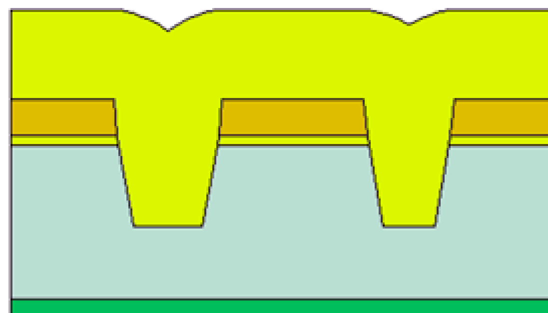


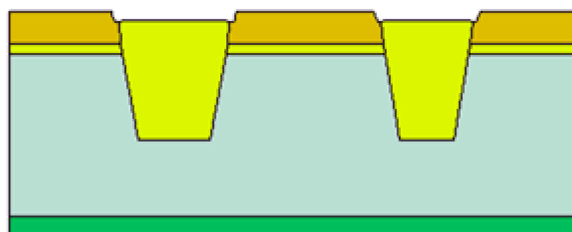
High-density plasma etch





Dry etch with side wall deposition





Local CMP planarization

PROCESS INTEGRATION IN 3D

Taurus-Topography is also used in 3D for quick process integration to build complicated multi-l structures. Figure 3a shows a typical 3D simulation of multiple SRAM cells. The simulation take the mask layout and process recipe as inputs. The original layout design is shown in Figure 3c. actual patterns of the materials on the wafer are altered by the photolithography processes. Fig 3d shows the result of the lithography simulation. In Figure 3b an enlarged view of the same simulation is shown to give better details.

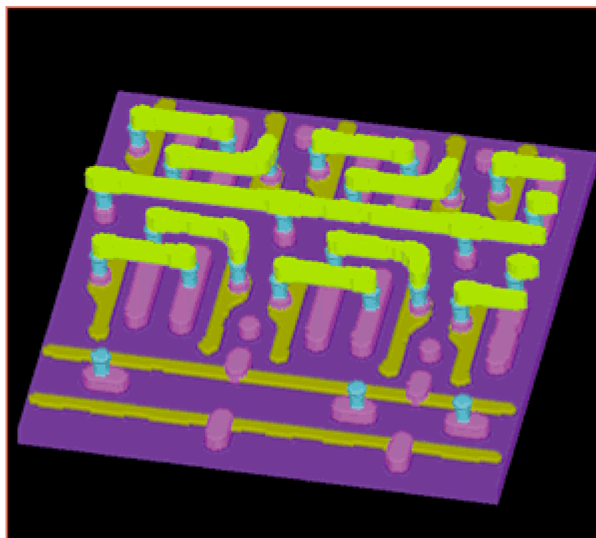


Figure 3a: Taurus-Topography 3D simulation of multiple SRAM cells

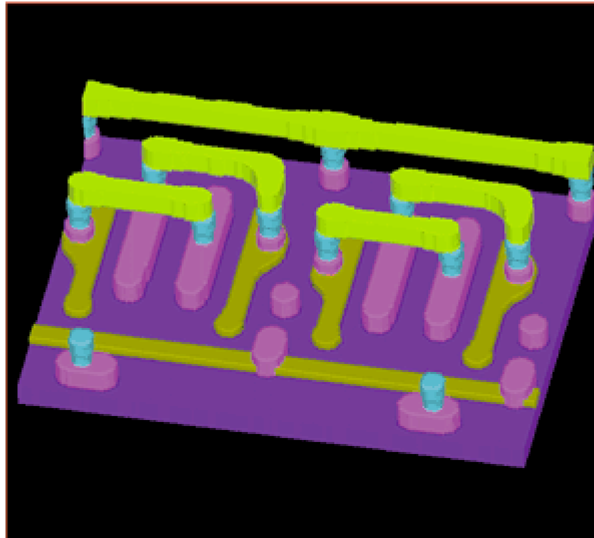


Figure 3b: Enlarged view of simulation

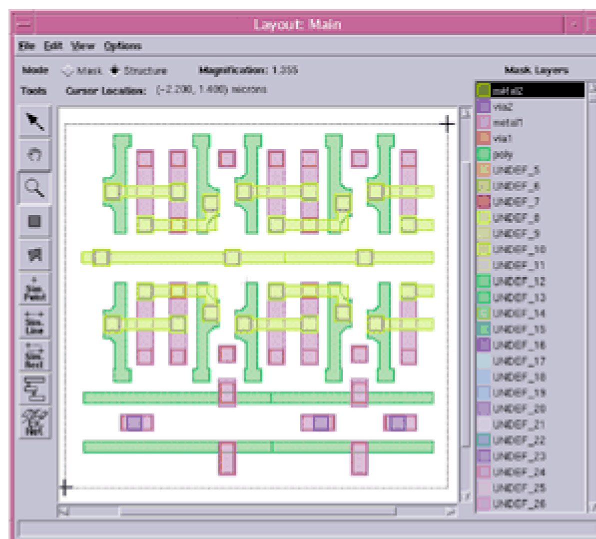


Figure 3c: Typical layout of SRAM cells

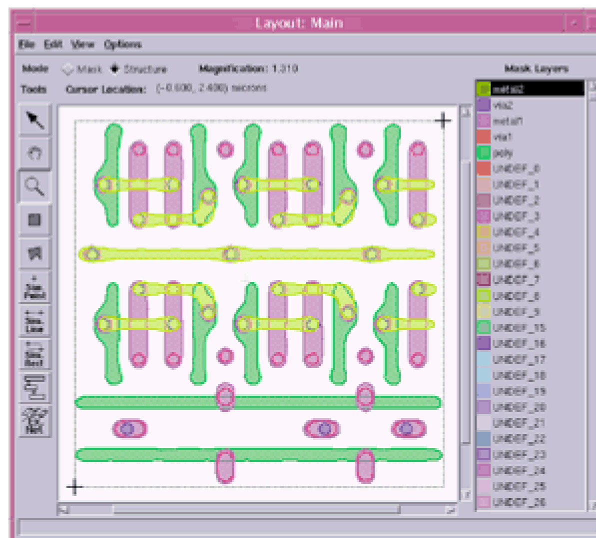


Figure 3d: Actual pattern on wafer after photolithography process

MISALIGNMENT STUDY OF A DRAM CELL

For the complex DRAM designs created for 64 Mbit and 256 Mbit chips, it is almost impossible
visualize the three-dimensional shape of the complete structure from the layout. A typical layou
stacked capacitor cell for a 64 Mbit DRAM is shown in Figure 4a. The three-dimensional structu
Figure 4b shows the DRAM cell after deposition and patterning the third polysilicon layer.

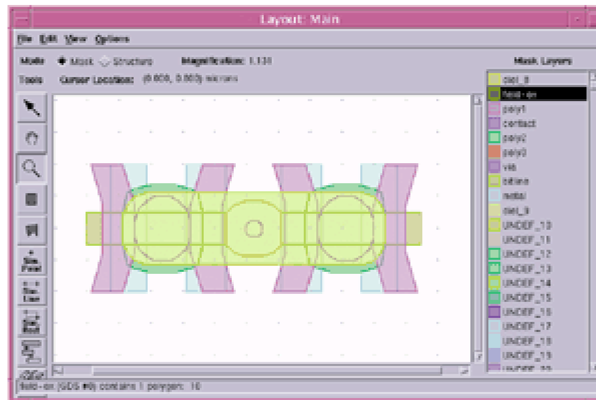


Figure 4a: Typical layout of a cylindrical DRAM cell

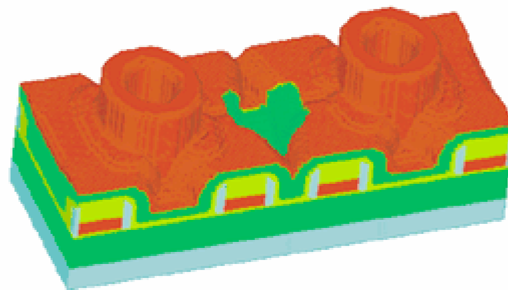


Figure 4b: 3D simulation of a cylindrical DRAM cell

Figure 4c: 2D cross-sectional view

Figure 4d: 2D cross-sectional view showing misalignment

Taurus-Topography is a powerful tool for performing "what-if" cross- section analysis. In Figure
cross section at the center of the DRAM cell shows the structure after deposition and patterning

the first metal layer. In Figure 4d, the result of a misalignment study is shown. In this case, the mask for the patterning of the second polysilicon layer and the layer for first metal contact to ac region have been misaligned. The effect of these process perturbations is revealed due to the short circuits between the ?rst and the second polysilicon layers and contact of the first met layer to the third poly layer.

Another very important application of Taurus-Topography simulation is to generate realistic three-dimensional geometries for parasitic extraction. An interface links Taurus-Topography an Raphael for integration of topography simulation, capacitance extraction and other related calculations. One example is the SRAM cell design and performance analysis. Figure 5a shows layout of a typical SRAM cell. Figure 5b shows the simulated final interconnect structure, which be used for subsequent parasitic extraction.

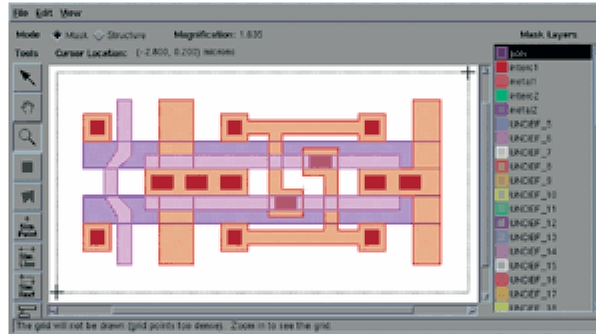


Figure 5a: 2D cross-sectional view

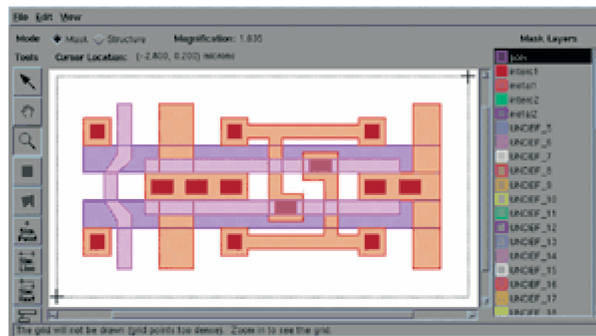


Figure 5b: 2D cross-sectional view

TAURUS-TOPOGRAPHY SPECIFICATIONS

PARTIAL LIST OF MODELS SUPPORTED BY TAURUS-TOPOGRAPHY

Standard models in Taurus-Topography allow for modeling of etch and deposition in a structure represents a cross section of an arbitrarily shaped structure composed of any number of mater These models include:

- Physical vapor deposition (PVD):
    - Isotropic, unidirectional and hemispherical.
- Low Pressure Chemical Vapor Deposition (LPCVD):
    - Re-emission and surface curvature effect.
- Atmospheric Pressure Chemical Vapor Deposition (APCVD):
    - Gas-phase diffusion and surface reaction.
    - Surface curvature effect.
- Plasma Characterization:
    - Monte Carlo sheath simulation.
    - Characterization of velocity (angular) and energy distribution of ions arriving at wa surface.
- Plasma Enhanced Chemical Vapor Deposition (PECVD):

- Ion-induced deposition.
- Thermally driven chemical vapor deposition that features re-emission.

- High-Density Plasma Chemical Vapor Deposition (HDP CVD):
  - Simultaneous deposition and ion milling effect.
  - Facet formation due to the angular dependency of sputter yield.
  - Re-deposition of sputtered materials.

- Reflow process.
- Spin deposition:
  - Series of initial spin, reflow and shrinking.

- Wet etch:
  - Isotropic and anisotropic.
  - Super-isotropic (larger lateral than vertical etch rates).

- Ion milling:
  - Physical sputtering by heavy incoming ions.
  - Hemispherical etch that features angular-distribution dependency.

- Reactive Ion Etch (RIE):
  - Ion-driven chemical etch.

- High-Density Plasma Etch:
  - Simultaneous reactive ion etch and physical sputtering.

- Plasma Dry Etch of polysilicon, silicon and oxide, etc.:
  - Simultaneous deposition of thin polymer side wall that results from gas phase rea and controls the etch profile as a blocking layer.

- Local CMP planarization.

PLATFORMS
Taurus-Topography supports the following operating systems:

- Sun SPARC Solaris 2.5.
- Hewlett-Packard HP-UX 10.20 (PA-RISC 1.1).

CONFIGURATIONS
Recommended minimum system requirements for UNIX workstations:

- Memory: 64 Mbytes.
- Disk Space: 100 Mbytes.

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