

## **SELECTED RECENT PUBLICATIONS**

### **BOOK:**

Albert Wang, *On-Chip ESD Protection for Integrated Circuits – An IC Design Perspective*, Kluwer Academic Publishers, Boston, 2002, ISBN: 0-7923-7647-1.

## **SELECTED TOPICAL PUBLICARIONS**

### **On-Chip ESD Protection for RF/AMS ICs:**

- L. Lin, X. Wang, H. Tang, Q. Fang, H. Zhao, Albert Wang, R. Zhan, H. Xie, C. Gill, B. Zhao, Y. Zhou, G. Zhang and X. Wang, "Whole-Chip ESD Protection Design Verification by CAD", **Invited**, *IEEE Proc. EOS/ESD Symp*, pp.28-37, Anaheim, CA, 2009.
- X. Wang, H. Tang, L. Lin, Q. Fang, H. Zhao, Albert Wang, G. Zhang, X. Wang, Y. Zhou, Lee Yang and H. Chen, "ESD Protection for RF/AMS ICs: Design and Optimization", **Invited**, *Proc. IEEE Intl. Conf. IC Design and Technology (ICICDT)*, pp25-28, Austin, May 2009.
- Albert Wang, L. Lin, X. Wang and H. Liu, "Emerging Challenges in ESD Protection for RF ICs in CMOS", **Invited**, *J. of Semiconductors*, 29(4), pp628-636, April 2008.
- X. Guan, X. Wang, L. Lin, G. Chen, Albert Wang, H. Liu, Y. Zhou, H. Chen, L. Yang and B. Zhao, "ESD-RFIC Co-Design Methodology", **Invited**, *Proc. IEEE RFIC*, pp467-470, Atlanta, 2008.
- X. Wang, L. Lin, X. Guan, G. Chen, Albert Wang, H. Liu, Y. Zhou, L. Yang, H. Chen and B. Zhao, "ESD-Sensitive LNA Design", *IEEE Proc. Asia-Pacific Symposium on Electromagnetic Compatibility (AP-EMC) and 19<sup>th</sup> International Zurich Symposium on Electromagnetic Compatibility*, pp. 156-159, 2008.
- L. Lin, J. Liu, X. Wang, Albert Wang, H. Liu and Y. Zhou, "3D Electro-Thermal Modeling for ESD protection structures in Sub-100nm CMOS", **Invited**, *Proc. IEEE International Nanoelectronics Conference (INEC)*, pp871-874, 2008.
- X. Guan, G. Chen, L. Lin, X. Wang, Albert Wang, L. Yang and B. Zhao, "A New ESD-Aware Power Amplifier Design Method", *Proc. IEEE ASICON*, pp1363-1366, 2007.
- Albert Wang, H. Feng, R. Zhan, H. Xie, G. Chen, Q. Wu, X. Guan, Z. Wang and C. Zhang, "A Review on RF ESD Protection Design", *IEEE Trans. Electron Devices*, Vol. 52, No. 7, pp. 1304-1311, July 2005.
- H. Xie, H. Feng, R. Zhan, Albert Wang, D. Rodriguez and D. Rice, "A New Low-Parasitic Polysilicon SCR ESD Protection Structure for RF ICs", *IEEE Electron Device Letters*, Vol. 26, No.2, pp.121-123, February 2005.
- R. Zhan, H. Feng, Q. Wu, H. Xie, X. Guan, G. Chen and Albert Z. Wang, "ESDInspector: A New Layout-level ESD Protection Circuitry Design

Verification Tool Using A Smart-Parametric Checking Mechanism”, *IEEE Trans. CAD of Integrated Circuits and Systems*, Vol. 23, No. 10, pp.1421-1428, October 2004.

- G. Chen, H. Feng, H. Xie, R. Zhan, Q. Wu, X. Guan, Albert Wang, K. Takasuka, S. Tamura, Z. Wang and C. Zhang, “Characterizing Diodes For RF ESD Protection”, *IEEE Electron Device Letters*, Vol. 25, No. 5, pp.323-325, May 2004.
- H. Feng, R. Zhan, G. Chen, Q. Wu and Albert Z. Wang, “Electrostatic Discharge Protection for RF Integrated Circuits: New ESD Design Challenges”, *Analog Integrated Circuits and Signal Processing, An International Journal*, Vol. 39, Issue 1, pp. 5-19, April 2004.
- R. Zhan, H. Feng, Q. Wu and Albert Wang, “ESDExtractor: A New Technology-Independent CAD Tool for Arbitrary ESD Protection Device Extraction,” *IEEE Trans. CAD of Integrated Circuits and Systems*, Vol. 22, No. 10, pp.1362-1370, October 2003.
- H. Feng, G. Chen, R. Zhan, Q. Wu, X. Guan, H. Xie, Albert Wang and R. Gafiteanu, “A Mixed-Mode ESD Protection Circuit Simulation-Design Methodology,” *IEEE J. Solid-State Circuits*, V38, N6, pp.995-1006, June 2003.
- H. Feng, R. Zhan, Q. Wu, G. Chen and Albert Wang, “RC-SCR: A Very-Low-Voltage ESD Protection Circuit in Plain CMOS,” *IEE Electronics Letters*, V38, N19, pp.1099-1100, September 2002.
- H. G. Feng, R. Y. Zhan, Q. Wu, G. Chen and Albert Z. Wang, “A Circular Under-Pad Multiple-Mode ESD Protection Structure for ICs,” *IEE Electronics Letters*, V38, N11, pp. 511 –513, May 2002.
- H. G. Feng, K. Gong, R. Zhan and Albert Wang, “A Novel all-Direction on-Chip Protection Circuit,” *IEICE Trans. Electron.*, Vol. E85-C, N3, pp.566-571, March 2002.
- K. Gong, H. Feng, R. Zhan and Albert Z. Wang, “A Study of Parasitic Effects of ESD Protection on RF ICs,” *IEEE Trans. Microwave Theory and Techniques*, V50, N1, pp.393-402, January 2002.
- H. Feng, R. Zhan, K. Gong and Albert Z. Wang, “A New Pad-Oriented Multiple-Mode ESD Protection Structure and Layout Optimization,” *IEEE Electron Device Letters*, V22, N10, pp.493-495, Oct. 2001.
- K. Gong, H. G. Feng, R. Y. Zhan and Albert Z. Wang, “ESD-Induced Circuit Performance Degradation in RFICs,” *Microelectronics Reliability*, V41, Issue 9-10, PERGAMON, Elsevier Science, pp.1379-1383, September-October 2001.
- Albert Z. Wang, H. G. Feng, K. Gong, R. Y. Zhan and J. Stine, “On-Chip ESD Protection Design for Integrated Circuits: an Overview for IC Designers,” *Microelectronics Journal*, Elsevier Science, V32, Issue 9, pp.733-747, September 2001.
- H. G. Feng, K. Gong, R. Zhan and Albert Wang, “A Pad-Oriented Novel Electrostatic Discharge Protection Structure For Mixed-Signal ICs,” in *Advances in Systems Science: Measurement, Circuits and Control*, Edited by

*N. Mastorakis and L. Pecorelli-Peres, Electrical and Computer Engineering Series, WSES Press, 2001, pp.159-163.*

- H. G. Feng, K. Gong, and Albert Z. Wang, "A Novel on-Chip Electrostatic Discharge Protection Design for RFIC's," *Microelectronics Journal*, V32, Issue 3, Elsevier Science, pp 189-195, March 2001.
- Albert Wang and C. Tsay, "On a Dual-Direction on-Chip Electrostatic Discharge Protection Structure," *IEEE Trans. Electron Devices*, V48, N5, pp.978-984, May 2001.
- Albert Wang and C. Tsay, "An on-Chip ESD Protection Circuit with Low Trigger-Voltage in BiCMOS Technology," *IEEE J. Solid-State Circuits*, V36, N1, pp.40-45, January 2001.
- Albert Wang, C. Tsay, and P. Deane, "A Study of NMOS Behaviors under ESD Stress: Simulation and Characterization," *Microelectronics Reliability*, V38, Issue 6-8, PERGAMON, Elsevier Science, pp.1183-1186, 1998.
- Albert Wang, H. Feng, R. Zhan, H. Xie, G. Chen and X. Guan, "RF ESD Protection for VDSM Si Technology", *Proc. ECS 5<sup>th</sup> Int'l Semiconductor Technology Conference (ECS-ISTC)*, 2006.
- G. Chen, H. Feng, Albert Wang and Y. Cheng, "Noise Analysis of ESD Structures and Impacts on a Fully-Integrated 5.5GHz LNA in 0.18 $\mu$ m SiGe BiCMOS", *Proc. IEEE 35<sup>th</sup> European Microwave Conference*, October 2005.
- R. Zhan, H. Xie, H. Feng and Albert Wang, "ESDZapper: A New Layout-level Verification Tool for Finding Critical Discharging Path under ESD Stress", *Proc. IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 79-82, 2005.
- H. Xie, R. Zhan and Albert Wang, "3D Electro-Thermal Modeling of GGNMOS ESD Protection Structure", *Proc. IEEE Asia-Pacific Conf. on Circuits and Systems (APC-CAS)*, pp.61-64, 2004.
- G. Chen and Albert Wang, "Evaluating RF ESD Protection Design: An Overview", *Proc. IEEE 11<sup>th</sup> International Symp. Physical & Failure Analysis of ICs (IPFA)*, pp205-208, 2004.
- G. Chen, H. Feng, H. Xie, R. Zhan, Q. Wu, X. Guan, Albert Wang, K. Takasuka, S. Tamura, Z. Wang and C. Zhang, "RF Characterization of ESD Protection Structures", *Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, pp.379-382, 2004.
- Albert Z. Wang, H. Feng, G. Chen, R. Zhan, H. Xie, Q. Wu and X. Guan, "Key Aspects For ESD Protection Design In ICs: Mixed-Mode Simulation And RF/Mixed-Signal ESD Protection," *IEEE 25<sup>th</sup> Int'l Conf. on ASIC (ASICON)*, pp.1000-1005, 2003.
- H. Feng, R. Zhan, Q. Wu, G. Chen, X. Guan, H. Xie and Albert Z. Wang, "Mixed-Mode ESD Protection Circuit Simulation-Design Methodology," *Proc. IEEE Int'l Symp. Circuits and Systems (ISCAS)*, V1, pp.652-655, 2003.
- H. Feng, R. Zhan, G. Chen, Q. Wu, X. Guan, H. Xie and Albert Wang, "Bonding-Pad-Oriented on-Chip ESD Protection Structures for ICs," *Proc. IEEE Int'l Symp. Circuits and Systems (ISCAS)*, V 4, pp.741-744, 2003.

- G. Chen, H. Feng and Albert Wang, "A Systematic Study of ESD Protection Structures for RF ICs," *Proc. IEEE Symp. RF Integrated Circuits (RFIC)*, pp.347-350, 2003.
- Albert Wang, "Recent Developments in ESD Protection for RF ICs," *Proc. IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, pp.171-178, 2003.
- Albert Z. Wang, H. Feng, R. Zhan, G. Chen and Q. Wu, "ESD Protection Design for RF Integrated Circuits: New Challenges," *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, pp.411-418, 2002.
- K. Gong, H. Feng, R. Zhan and Albert Z. Wang, "ESD-Induced Circuit Performance Degradation in RFICs," *IEEE Proc. European Symp. Reliability of Electron Devices Failure Physics & Analysis (ESREF)*, pp.1379-1383, 2001.
- H. G. Feng, K. Gong, R. Zhan and Albert Wang, "A Pad-Oriented Novel Electrostatic Discharge Protection Structure For Mixed-Signal ICs," *Proc. WSES/IEEE Conferences: 5<sup>th</sup> Circuits, Systems, Communications & Computers*, pp.3421-3425, 2001.
- H. G. Feng, K. Gong, R. Zhan and Albert Wang, "A Novel all-Direction on-Chip Protection Circuit," *Proc. IEEE/IEICE Int'l Symp. Signals, Systems, and Electronics (ISSSE)*, pp.118-121, 2001.
- H. G. Feng, K. Gong and Albert Wang, "An ESD Protection Circuit for Mixed-Signal ICs," *Proc. IEEE CICC*, pp.493-496, 2001.
- H. G. Feng, K. Gong and Albert Wang, "A New Integrated Metal-Semiconductor Simulation Methodology for on-Chip Electrostatic Discharge Protection Design Optimization", *Proc. IEEE/IFIP World Computer Congress Int'l Conference on Design Automation*, pp.81-85, 2000.
- H. G. Feng, K. Gong and Albert Wang, "A Comparison Study of ESD Protection for RFIC's: Performance vs. Parasitics," *Proc. IEEE RFIC Symp.*, pp.235-238, 2000.
- Albert Z. Wang, "A New Design for Complete on-Chip ESD Protection," *Proc. IEEE Custom Integrated Circuits Conference*, pp. 87-90, 2000.
- Albert Z. Wang and C. H. Tsay, "A Compact Square-Cell ESD Structure for BiCMOS ICs," *Proc. IEEE BCTM*, pp. 46-49, 1999.
- Albert Wang, C. Tsay and Q. Shan, "A Novel Dual-Direction IC ESD Protection Device," *Proc. IEEE 7<sup>th</sup> Int'l Symp. Physical and Failure Analysis of Integrated Circuits*, pp.151-155, 1999.
- Albert Wang, C. Tsay, J. Bielawski and L. DeClue, "Design Optimization of a Practical ESD Protection Circuit by CAD: A Case Study," *Proc. IEEE 13<sup>th</sup> UGIM Symp.*, pp. 116-119, 1999.
- Albert Wang and C. Tsay, "A Low-Triggering Circuitry for Dual-Direction ESD Protection," *Proc. IEEE Custom Integrated Circuits Conference*, pp 139-142, 1999.
- Albert Wang, C. Tsay, A. Lele and P. Deane, "A Study of NMOS Behaviors under ESD Stress: Simulation and Characterization," *Proc. IEEE 9<sup>th</sup> European Symp. Reliability of Electron Devices Failure Physics & Analysis*, pp.151-155, 1998.

### **RF Inductors:**

- C. Yang, F. Liu, X. Wang, J. Zhan, Albert Wang, T. Ren, L. Liu, H. Long, Z. Wu, X. Li, "Investigation of on-Chip Soft-Ferrite-Integrated Inductors for RF ICs — Part I: Design and Simulation", *IEEE Trans. Electron Devices*, Vol. 56, No. 12, pp. 3133-3140, December 2009.
- C. Yang, F. Liu, X. Wang, J. Zhan, Albert Wang, T. Ren, L. Liu, H. Long, Z. Wu, X. Li, "Investigation of on-Chip Soft-Ferrite-Integrated Inductors for RF ICs — Part II: Experiments", *IEEE Trans. Electron Devices*, Vol. 56, No. 12, pp. 3141-3148, December 2009.
- F. Zhang, Z. Wang, X. Wang, H. Tang, Q. Fang, Albert Wang, W. Chen, L. Yang, B. Zhao, G. Zhang, and X. Wang, "Design Optimization and Modeling of on-Chip RF Inductors in 0.13 $\mu$ m and 90nm Standard CMOS", *Proc. IEEE MWSCAS*, pp.975-978, Cancun, Mexico, 2009.
- C. Yang, T. Ren, I. Liu, J. Zhan, X. Wang, Albert Wang, Z. Wu and X. Li, "on-Chip Soft-Ferrite-Integrated Inductors for RF IC", *Proc. IEEE Transducers*, pp. 785-788, Denver, June 2009.
- C. Yang, F. Liu, T. Ren, I. Liu, J. Zhan and Albert Wang, "Soft-Ferrite-Film Integration for on-Chip RF Passive Elements", *Proc. International Conference on Communication Technology and VLSI Design (CommV09)*, Oct., 2009.
- C. Yang, T. Ren, L. Liu, Y. Yuan, Albert Wang, and X. Wang, "Ferrite-integrated on-chip RF solenoid inductor," 7th IEEE Conference on Sensors (SENSORS), Lecce, Italy, pp. 1040-1043, Oct. 2008.
- Y. Yuan, C. Yang, T. Ren, J. Zhan, L. Liu and Albert Wang, "Design and Simulation of on-Chip Magnetic Inductors for RF ICs," *Proc. IEEE ICSICT*, *IEEE 978-1-4244-2186-2/08*, pp. 523-526, 2008.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang, and Z. Yue, "Ferrite-Partially-Filled on-Chip RF Inductor Fabricated Using Low-Temperature Nano-Powder-Mixed-Photoresist Filling Technique for Standard CMOS", *IEEE International Electron Device Meeting (IEDM) Tech. Digest*, pp1038-1040, 2007.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang and H. Feng, "Ferrite-Integrated on-Chip Inductors for RF ICs ", *IEEE Electron Device Letters*, Vol. 28, No. 7, pp652-655, July 2007
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang and H. Feng, "Ferrite-Integrated on-Chip Inductors for RF ICs ", *IEEE Electron Device Letters*, Vol. 28, No. 7, pp652-655, July 2007.
- F. Liu, C. Yang, T. Ren, Albert Wang, J. Yu and L. Liu, "NiCuZn Ferrite Thin Films Grown by a sol-gel Method and Rapid Thermal Annealing," *J. of Magnetism and Magnetic Materials*, V309, Issue 1, pp.17-21, March 2007.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang and H. Feng, "Magnetic film inductors for RF IC", **Invited**, *Proc. ECS Int'l Semiconductor Technology Conference (ECS-ISTC)*, pp447-462, 2007. 2<sup>nd</sup> Place, **Best Student Paper Award**.

- C. Yang, F. Liu, T. Ren, L. Liu, H. Feng, Albert Wang and H. Long, "Fully Integrated Ferrite-Based Inductors for RF ICs", *Sensors & Actuators: A. Physical*, A 130-131, p365-370, 2006.
- F. Liu, T. Ren, C. Yang, L. Liu, Albert Wang, and J. Yu, "NiCuZn Ferrite Thin Films for RF Integrated Inductors," *Materials Letter*, Vol. 60, pp. 1403-1406, 2006.
- T. Ren, C. Yang, F. Liu, L. Liu, Albert Z. Wang and X. Zhang, "Equivalent Circuit Analysis of an RF Integrated Inductor with Ferrite Thin-Film," *Journal of Semiconductors*, Vol. 27, pp. 511-515, 2006.
- C. Yang, F. Liu, T. Ren, L. Liu, H. Feng, Z. Albert Wang, H. Long and J. Yu, "RF Integrated Inductor with CoZrO Ferrite Thin Film," *Journal of Semiconductors*, Vol. 26, pp. 2208-2212, 2005.
- H. Long, Z. Feng, H. Feng, Albert Wang, Tianling, Ren, Junbo Bao, Feng Liu, Chen Yang, Xiao Zhang, "A New Modeling Technique for Simulating 3D Arbitrary Conductor-Magnet Structures for RFIC Applications", *IEEE Tans. Electron Devices*, Vol. 52, No. 7, pp. 1354-1363, July 2005.
- H. Long, Z. Feng, H. Feng and Albert Wang, "A Novel Accurate PEEC-based 3D Modeling Technique for RF Devices of Arbitrary Conductor-Magnet Structure," *Microwave and Optical Technology Letters*, V38, Issue 3, Wiley & Sons, pp.237-240, August 2003.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang and Z. Yue, "Ni-Zn Ferrite Film Coated on-Chip RF Inductor Fabricated by A Novel Powder-Mixed-Photoresist Spin-Coating Technique", *Proc. IEEE MTT-S Int'l Microwave Symposium (IMS)*, pp465-468, 2007.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan and Albert Wang, "Magnetic film inductors for RF IC", *Proc. ECS Int'l Semiconductor Technology Conference (ECS-ISTC)*, pp447-462, 2007.
- C. Yang, F. Liu, T. Ren, L. Liu and Albert Z. Wang, "On-Chip Integrated Inductors with Ferrite Thin-Films for RFIC", *Tech. Digest, IEEE International Electron Devices Meeting (IEDM)*, pp225-228, 2006.
- C. Yang, F. Liu, T. Ren, L. Liu and Albert Z. Wang, "On-Chip Integrated Inductors with Ni-Zn-Cu-Fe and Y-Bi-Fe Thin-Films for RF IC", *Proc. 34<sup>th</sup> IEEE European Solid-State Device Research Conf (ESSDERC)*, pp. 194-197, September 2006.
- F. Liu, C. Yang, T. L. Ren, L. T. Liu, H. G. Feng, Albert Z. Wang, H. B. Long and J Yu, "Fully Integrated Ferrite-Based Inductors for RF ICs", *Proc. IEEE International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, Vol 1, pp.895 - 898, 2005.
- H. Long, Z. Feng, H. Feng, Albert Wang and T. Ren, "L-SIMULATOR: A MAGPEEC-Based new CAD Tool for Simulating Magnetic-Enhanced IC Inductors of 3D Arbitrary Geometry", *Proc. IEEE International Symp. Circuits and Systems (ISCAS)*, Vol 5, pp. V-233/237, 2004.
- H. Long, Z. Feng, H. Feng and Albert Wang, "magPEEC: Extended PEEC Modeling for 3D Arbitrary Electro-Magnetic Devices with Application for M-Cored Inductors," *Proc. IEEE Symp. RF Integrated Circuits (RFIC)*, pp.251-254, 2003.

- H. Feng, G. Jelodin, K. Gong, R. Zhan, Q. Wu, C. Chen and Albert Wang, "Super Compact RFIC Inductors in 0.18 $\mu$ m CMOS with Copper Interconnects," *Proc. IEEE Microwave Symposium Digest, 2002, IEEE MTT-S International, V1*, pp. 553 –556, 2002.

**RF/AMS ESD Protection Circuit Design Method:**

- X. Guan, X. Wang, L. Lin, G. Chen, Albert Wang, H. Liu, Y. Zhou, H. Chen, L. Yang and B. Zhao, "ESD-RFIC Co-Design Methodology", **Invited**, *Proc. IEEE RFIC*, pp467-470, Atlanta, 2008.
- X. Wang, L. Lin, X. Guan, G. Chen, Albert Wang, H. Liu, Y. Zhou, L. Yang, H. Chen and B. Zhao, "ESD-Sensitive LNA Design", *IEEE Proc. Asia-Pacific Symposium on Electromagnetic Compatibility (AP-EMC) and 19<sup>th</sup> International Zurich Symposium on Electromagnetic Compatibility*, pp. 156-159, 2008.
- L. Lin, J. Liu, X. Wang, Albert Wang, H. Liu and Y. Zhou, "3D Electro-Thermal Modeling for ESD protection structures in Sub-100nm CMOS", **Invited**, *Proc. IEEE International Nanoelectronics Conference (INEC)*, pp871-874, 2008.
- X. Guan, G. Chen, L. Lin, X. Wang, Albert Wang, L. Yang and B. Zhao, "A New ESD-Aware Power Amplifier Design Method", *Proc. IEEE ASICON*, pp1363-1366, 2007.
- H. Xie, R. Zhan, H. Feng, G. Chen, Albert Wang and R. Gafiteanu, "A 3D Mixed-Mode ESD Protection Circuit Simulation-Design Methodology", *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, pp243-246, 2004.
- R. Zhan, H. Feng, Q. Wu, H. Xie, X. Guan, G. Chen and Albert Z. Wang, "ESDInspector: A New Layout-level ESD Protection Circuitry Design Verification Tool Using A Smart-Parametric Checking Mechanism", *IEEE Trans. CAD of Integrated Circuits and Systems, Vol. 23, No. 10*, pp.1421-1428, October 2004.
- H. Feng, G. Chen, R. Zhan, Q. Wu, X. Guan, H. Xie, Albert Wang and R. Gafiteanu, "A Mixed-Mode ESD Protection Circuit Simulation-Design Methodology," *IEEE J. Solid-State Circuits, V38, N6*, pp.995-1006, June 2003.
- R. Zhan, H. Feng, Q. Wu and Albert Wang, "ESDExtractor: A New Technology-Independent CAD Tool for Arbitrary ESD Protection Device Extraction," *IEEE Trans. CAD of Integrated Circuits and Systems, Vol. 22, No. 10*, pp.1362-1370, October 2003.
- Albert Wang and C. Tsay, "A Novel Design Methodology Using Simulation for on-chip ESD Protection for Integrated Circuits," *Proc. IEEE Intl. Conf. Solid-State & IC Technology*, pp.509-512, 1998.

**RF IC Chips:**

- B. Qin, X. Wang, H. Chen, Albert Wang, Y. Hao, L. Yang and B. Zhao, "A Single-Chip 33pJ/pulse 5<sup>th</sup>-Derivative Gaussian Based IR-UWB Transmitter in 0.13 $\mu$ m CMOS", *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp.401-404, Taipei, May 2009.
- B. Qin, X. Wang, H. Chen, Albert Wang and B. Zhao, "A Programmable 1.8pJ/b Gaussian Pulse Generator for Impulse UWB Transceivers in 90nm CMOS", *Proc. IEEE Radio and Wireless Symposium (RWS)*, pp.498-501, San Diego, 2009. **(Best Student Paper candidate)**
- X. Wang, B. Qin, H. Xie, L. Lin, H. Tang, Q. Fang, H. Zhao, S. Wang, Albert Wang, H. Chen, B. Zhao, Y. Zhou, L. Yang and G. Zhang, "FCC-EIRP-Aware UWB Pulse Generator Design Approach", **Invited**, *Proc. IEEE Intl. Conf. Ultra Wideband (ICUWB)*, pp.592-596, Vancouver, Canada, 2009.
- H. Xie, X. Wang, L. Lin, H. Tang, Q. Fang, H. Zhao, S. Wang, F. Yao, Albert Wang and Y. Zhou, "A 52mW 3.1-10.6GHz Fully Integrated Correlator for IR-UWB Transceivers in 0.18 $\mu$ m CMOS", in press, *IEEE Trans. Industrial Electronics*, 2009.
- X. Guan, X. Wang, Albert Wang and B. Zhao, "A 3V 110 $\mu$ W 3.1ppm/C curvature-compensated CMOS bandgap reference", in press, *Analog Integrated Circuits and Signal Processing, An International Journal*, DOI#: 0.1007/s10470-009-9333-7, 2009.
- Bo Qin, Hongyi Chen, Xin Wang and Albert Wang, "An Ultra Low-Power FCC-Compliant 5<sup>th</sup>-Derivative Gaussian Pulse Generator for IR-UWB Transceiver", in press, *Journal of Electronics*, 2009.
- B. Qin, X. Wang, H. Xie, L. Lin, H. Tang, Albert Wang, H. Chen, B. Zhao, L. Yang and Y. Zhou, "1.8pJ/pulse Programmable Gaussian Pulse Generator for Full-Band Non-Carrier Impulse UWB Transceivers in 90nm CMOS", in press, *IEEE Trans. Industrial Electronics*, 2009.
- B. Qin, X. Wang, H. Chen, Albert Wang and B. Zhao, "A Tunable 2.4pJ/b 1<sup>st</sup>-Order Derivative Gaussian Pulse Generator for Impulse UWB Transceivers in 0.13 $\mu$ m CMOS," *Proc. IEEE ICSICT*, pp1544-1547, 2008.
- H. Xie, X. Wang, Albert Wang, B. Zhao, Y. Zhou, B. Qin, H. Chen and Z. Wang, "A Varying Pulse Width 5<sup>th</sup>-Derivative Gaussian Pulse Generator for UWB Transceivers in CMOS", *Proc. IEEE Radio and Wireless Symposium (RWS)*, pp171-174, 2008.
- X. Guan, X. Wang, L. Lin, G. Chen, Albert Wang, H. Liu, Y. Zhou, H. Chen, L. Yang and B. Zhao, "ESD-RFIC Co-Design Methodology", **Invited**, *Proc. IEEE RFIC*, pp467-470, Atlanta, 2008.
- X. Wang, L. Lin, X. Guan, G. Chen, Albert Wang, H. Liu, Y. Zhou, L. Yang, H. Chen and B. Zhao, "ESD-Sensitive LNA Design", *IEEE Proc. Asia-Pacific Symposium on Electromagnetic Compatibility (AP-EMC) and 19<sup>th</sup> International Zurich Symposium on Electromagnetic Compatibility*, pp. 156-159, 2008.
- L. Lin, J. Liu, X. Wang, Albert Wang, H. Liu and Y. Zhou, "3D Electro-Thermal Modeling for ESD protection structures in Sub-100nm CMOS", **Invited**, *Proc. IEEE International Nanoelectronics Conference (INEC)*, pp871-874, 2008.



- X. Wang, H. Xie, Albert Wang, B. Qin, H. Chen, S. Qiao, Y. He and Y. Zhou, "Simulation Design of A New 3.1-10.6GHz Single-Full-Band Non-Carrier Pulse-Based Ultra Wideband System", *Proc. IEEE ASICON*, pp834-837, October 2007.
- X. Guan, G. Chen, L. Lin, X. Wang, Albert Wang, L. Yang and B. Zhao, "A New ESD-Aware Power Amplifier Design Method", *Proc. IEEE ASICON*, pp1363-1366, 2007.
- H. Xie, X. Wang, Albert Wang, B. Qin, H. Chen, B. Zhao and L. Yang, "A Broadband CMOS Multiplier-Based Correlator for IR-UWB Transceiver SoC", *Proc. IEEE RFIC*, pp493-496, 2007.
- H. Xie, X. Wang, Albert Wang, B. Qin, H. Chen, Y. Zhou and B. Zhao, "A Varying Pulse Width Second Order Derivative Gaussian Pulse Generator for UWB Transceivers in CMOS", *Proc. IEEE Int'l Symp. Circuits and Systems (ISCAS)*, pp2794-2797, 2007.
- H. Xie, X. Wang, Albert Wang, Z. Wang and C. Zhang, "A Fully-Integrated Low-Power 3.1-10.6GHz UWB LNA in 0.18 $\mu$ m CMOS", *Proc. IEEE Radio and Wireless Symposium (RWS)*, pp.197-200, January 2007.
- H. Xie, X. Wang, Albert Wang, B. Qin, H. Chen and B. Zhao, "An Ultra Low-Power Low-Cost Gaussian Impulse Generator for UWB Applications", *Proc. IEEE Int'l Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1817-1820, 2006.
- H. Xie, S. Fan, X. Wang, Albert Wang, Z. Wang and H. Chen, "A Pulse-Based Non-Carrier 7.5GHz UWB Transceiver SoC with on-Chip ADC", *Proc. IEEE Int'l Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1804-1807, 2006.
- H. Xie, S. Fan, X. Wang, Albert Wang, Z. Wang and H. Chen, "A Pulse-Based Full-Band UWB Transceiver SoC in 0.18 $\mu$ m SiGe BiCMOS", *Proc. IEEE International SoC Conference*, pp.73-76, 2006.
- H. Xie, S. Fan, X. Wang and Albert Wang, "An Ultra-Low Power Pulse-Based UWB Transceiver SoC", *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, paper#: 3248, pp.111, 2006.
- X. Guan, H. Feng, Albert Wang and L. Yang, "A New Circuit Model for Designing Fully Integrated Class-A Power Amplifier", *Proc. 25<sup>th</sup> IEEE Int'l Conference on Microelectronics (MIEL)*, pp. 409-412, 2006.
- H. Xie and Albert Wang, "A Fine-Tuned Low-Power LNA for Lower-Band UWB Transceiver", *Proc. IEEE International Conference on Electron Devices and Solid-State Circuits*, pp.217-220, 2005.
- Albert Wang, X. Guan, H. Feng, Q. Wu, R. Zhan and L. Yang, "A 2.4 GHz Fully Integrated Class-A Power Amplifier In 0.35 $\mu$ m SiGe BiCMOS Technology", *Proc. IEEE Int'l Conf. on ASIC (ASICON)*, pp.360-363, 2005.
- H. Xie, X. Wang and Albert Wang, "A Fully-Integrated Fine-Tuned Low-Power 3.1-10.6GHz UWB LNA in 0.18 $\mu$ m SiGe BiCMOS", *Proc. IEEE 35<sup>th</sup> European Microwave Conference, V3*, pp. 1718–1722, 2005.

- G. Chen, H. Feng, Albert Wang and Y. Cheng, "Noise Analysis of ESD Structures and Impacts on a Fully-Integrated 5.5GHz LNA in 0.18 $\mu$ m SiGe BiCMOS", *Proc. IEEE 35<sup>th</sup> European Microwave Conference*, October 2005.
- Albert Wang, H. Feng, Q. Wu, X. Guan and R. Zhan, "A 2.45GHz Wide Tuning Range VCO Using MOS Varactor in 0.35 $\mu$ m SiGe BiCMOS Technology", *Proc. IEEE International Symp. Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications (MAPE)*, pp.10-13, 2005.
- H. Feng, Q. Wu, X. Guan, R. Zhan, Albert Wang and L. W. Yang, "A 5GHz Dual-Band Sub-Harmonic Direct Down-Conversion Mixer In 0.35 $\mu$ m SiGe BiCMOS", *Proc. IEEE International Symp. on Circuits and Systems (ISCAS)*, pp.4807-4810, 2005.
- H. Feng, H. Xie, Albert Wang, Y. Cheng and S. Lloyd, "A Full-Monolithic LNA in 0.18 $\mu$ m SiGe: Performance Variation Due to ESD Protection", *Proc. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Vol 2*, pp.1226 – 1229, 2004.
- H. Feng, Albert Wang and L. Yang, "A New 5.5GHz LNA with Gain Control and Turn-off Control for Dual-Band WLAN Systems", *Proc. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Vol 2*, pp.1248 - 1251, 2004.
- Albert Wang, "Recent Developments in ESD Protection for RF ICs," *Proc. IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, pp.171-178, 2003.
- H. G. Feng, K. Gong and Albert Wang, "A Comparison Study of ESD Protection for RFIC's: Performance vs. Parasitics," *Proc. IEEE RFIC Symp.*, pp.235-238, 2000.

### **Mixed-Signal IC Chips**

- X. Wang, B. Qin, H. Xie, L. Lin, H. Tang, Q. Fang, H. Zhao, S. Wang, Albert Wang, H. Chen, B. Zhao, Y. Zhou, L. Yang and G. Zhang, "FCC-EIRP-Aware UWB Pulse Generator Design Approach", **Invited**, *Proc. IEEE Intl. Conf. Ultra Wideband (ICUWB)*, pp.592-596, Vancouver, Canada, 2009.
- Q. Wu, S Fan, Albert Wang, K. Takasuka and S. Takeuchi, "An Optimized Pipelined-Subranging ADC Architecture", *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, paper#: 3249, pp.62, 2006.
- X. Guan, H. Feng, Albert Wang, A. Ishikawa, S. Tamura, K. Takasuka, Z. Wang and C. Zhang "A 3V 110uW 3.1ppm/ $^{\circ}$ C Curvature-Compensated CMOS Bandgap Reference", *Proc. IEEE Int'l Symp. on Circuits and Systems (ISCAS)*, pp.2861-2864, 2006.
- Q. Wu and Albert Wang, "A 12bits/200MHz Resolution/Sampling/Power-Optimized ADC In 0.25 $\mu$ m SiGe BiCMOS", *Proc. IEEE International Symp. on Circuits and Systems (ISCAS)*, pp.6174-6177, 2005.

### **CAD & Modeling:**

- L. Lin, X. Wang, H. Tang, Q. Fang, H. Zhao, Albert Wang, R. Zhan, H. Xie, C. Gill, B. Zhao, Y. Zhou, G. Zhang and X. Wang, "Whole-Chip ESD Protection Design Verification by CAD", **Invited**, *IEEE Proc. EOS/ESD Symp*, pp.28-37, Anaheim, CA, 2009.
- L. Lin, J. Liu, X. Wang, A. Wang, H. Liu and Y. Zhou, "3D Electro-Thermal Modeling for ESD protection structures in Sub-100nm CMOS", **Invited**, to appear, *Proc. IEEE International Nanoelectronics Conference (INEC)*, March, 2008.
- R. Zhan, H. Feng, Q. Wu, H. Xie, X. Guan, G. Chen and Albert Z. Wang, "ESDInspector: A New Layout-level ESD Protection Circuitry Design Verification Tool Using A Smart-Parametric Checking Mechanism", *IEEE Trans. CAD of Integrated Circuits and Systems*, Vol. 23, No. 10, pp.1421-1428, October 2004.
- R. Zhan, H. Feng, Q. Wu and Albert Wang, "ESDExtractor: A New Technology-Independent CAD Tool for Arbitrary ESD Protection Device Extraction," *IEEE Trans. CAD of Integrated Circuits and Systems*, Vol. 22, No. 10, pp.1362-1370, October 2003.
- H. Long, Z. Feng, H. Feng, Albert Wang, Tianling, Ren, Junbo Bao, Feng Liu, Chen Yang, Xiao Zhang, "A New Modeling Technique for Simulating 3D Arbitrary Conductor-Magnet Structures for RFIC Applications", *IEEE Tans. Electron Devices*, Vol. 52, No. 7, pp. 1354-1363, July 2005.
- H. Long, Z. Feng, H. Feng and Albert Wang, "A Novel Accurate PEEC-based 3D Modeling Technique for RF Devices of Arbitrary Conductor-Magnet Structure," *Microwave and Optical Technology Letters*, V38, Issue 3, Wiley & Sons, pp.237-240, August 2003.
- X. Guan, H. Feng, Albert Wang and L. Yang, "A New Circuit Model for Designing Fully Integrated Class-A Power Amplifier", *Proc. 25<sup>th</sup> IEEE Int'l Conference on Microelectronics (MIEL)*, pp. 409-412, 2006.
- H. Xie, R. Zhan and Albert Wang, "3D Electro-Thermal Modeling for on-Chip ESD Protection Structures", *Proc. IEEE International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, pp. 877-880, 2005.
- R. Zhan, H. Xie, H. Feng and Albert Wang, "ESDZapper: A New Layout-level Verification Tool for Finding Critical Discharging Path under ESD Stress", *Proc. IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 79-82, 2005.
- H. Xie, R. Zhan and Albert Wang, "3D Electro-Thermal Modeling of GGNMOS ESD Protection Structure", *Proc. IEEE Asia-Pacific Conf. on Circuits and Systems (APC-CAS)*, pp.61-64, 2004.
- H. Xie, R. Zhan, Albert Wang and R. Gafiteanu, "Real 3D Electro-Thermal Simulation and Analysis for ESD Protection Structures", *Proc. IEEE International Caracas Conference on Devices, Circuits and Systems (ICCDACS)*, pp61-64, 2004.

- H. Long, Z. Feng, H. Feng, Albert Wang and T. Ren, “L-SIMULATOR: A MAGPEEC-Based new CAD Tool for Simulating Magnetic-Enhanced IC Inductors of 3D Arbitrary Geometry”, *Proc. IEEE International Symp. Circuits and Systems (ISCAS), Vol 5*, pp. V-233/237, 2004.
- R. Zhan, H. Feng, H. Xie and Albert Wang, ‘ESDInspector: A New Layout-level ESD Protection Circuitry Design Verification Tool Using a Smart-Parametric Checking Mechanism’, *Proc. IEEE International Symp. Circuits and Systems (ISCAS), Vol 5*, pp. V217-220, 2004.
- R. Zhan, H. Feng, Q. Wu, X. Guan, G. Chen, H. Xie and Albert Wang, “Concept and Extraction Method of ESD-Critical Parameters for Function-Based Layout Level ESD Protection Circuit Design Verification”, *Proc. IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, pp.710-712, 2004.
- R. Zhan, H. Feng, G. Chen, Q. Wu, X. K. Guan and Albert Wang, “A New Technology-independent CAD Tool For ESD Protection Device Extraction – ESDEXtractor,” *Proc. IEEE/ACM Int’l Conf. Computer Aided Design (ICCAD)*, pp.510-513, 2002.
- R. Zhan, H. Feng, Q. Wu, G. Chen, X. Guan and Albert Wang, “A New Algorithm for ESD Protection Device Extraction Based on Subgraph Isomorphism,” *Proc. IEEE Asia-Pacific Conference on Circuits and Systems (APC-CAS)*, pp.361-366, 2002.

**Misc. Topics:**

- L. Zhang, R. Huang, D. Gao, D. Wu, Y. Kuang, P. Tang, W. Ding, Albert Wang and Y. Wang, “Unipolar Resistive Switch Based on Silicon Monoxide Realized by CMOS Technology”, *IEEE Electron Device Letters, Vol. 30, No. 8, August 2009*, pp.870-872.
- L. Zhang, R. Huang, Albert Wang, D. Wu, R. Wang, Y. Kuang, “The Parasitic Effects Induced by the Contact in RRAM with MIM Structure“, *Proc. IEEE ICSICT*, pp932-935, 2008.

**SELECTED RECENT PUBLICATIONS**  
(as Principal Author)

**Journal Papers:**

- C. Yang, F. Liu, X. Wang, J. Zhan, Albert Wang, T. Ren, L. Liu, H. Long, Z. Wu, X. Li, “Investigation of on-Chip Soft-Ferrite-Integrated Inductors for RF ICs — Part I: Design and Simulation”, *IEEE Trans. Electron Devices, Vol. 56, No. 12*, pp. 3133-3140, December 2009.
- C. Yang, F. Liu, X. Wang, J. Zhan, Albert Wang, T. Ren, L. Liu, H. Long, Z. Wu, X. Li, “Investigation of on-Chip Soft-Ferrite-Integrated Inductors for RF ICs — Part II: Experiments”, *IEEE Trans. Electron Devices, Vol. 56, No. 12*, pp. 3141-3148, December 2009.

- H. Xie, X. Wang, L. Lin, H. Tang, Q. Fang, H. Zhao, S. Wang, F. Yao, Albert Wang and Y. Zhou, "A 52mW 3.1-10.6GHz Fully Integrated Correlator for IR-UWB Transceivers in 0.18 $\mu$ m CMOS", in press, *IEEE Trans. Industrial Electronics*, 2009.
- L. Zhang, R. Huang, D. Gao, D. Wu, Y. Kuang, P. Tang, W. Ding, Albert Wang and Y. Wang, "Unipolar Resistive Switch Based on Silicon Monoxide Realized by CMOS Technology", *IEEE Electron Device Letters*, Vol. 30, No. 8, August 2009, pp.870-872.
- X. Guan, X. Wang, Albert Wang and B. Zhao, "A 3V 110 $\mu$ W 3.1ppm/C curvature-compensated CMOS bandgap reference", in press, *Analog Integrated Circuits and Signal Processing, An International Journal*, DOI#: 0.1007/s10470-009-9333-7, 2009.
- Bo Qin, Hongyi Chen, Xin Wang and Albert Wang, "An Ultra Low-Power FCC-Compliant 5th-Derivative Gaussian Pulse Generator for IR-UWB Transceiver", in press, *Journal of Electronics*, 2009.
- B. Qin, X. Wang, H. Xie, L. Lin, H. Tang, Albert Wang, H. Chen, B. Zhao, L. Yang and Y. Zhou, "1.8pJ/pulse Programmable Gaussian Pulse Generator for Full-Band Non-Carrier Impulse UWB Transceivers in 90nm CMOS", in press, *IEEE Trans. Industrial Electronics*, 2009.
- Albert Wang, L. Lin, X. Wang and H. Liu, "Emerging Challenges in ESD Protection for RF ICs in CMOS", **Invited**, *J. of Semiconductors*, 29(4), pp628-636, April 2008.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang and H. Feng, "Ferrite-Integrated on-Chip Inductors for RF ICs ", *IEEE Electron Device Letters*, Vol. 28, No. 7, pp652-655, July 2007
- F. Liu, C. Yang, T. Ren, Albert Wang, J. Yu and L. Liu, "NiCuZn Ferrite Thin Films Grown by a sol-gel Method and Rapid Thermal Annealing," *J. of Magnetism and Magnetic Materials*, V309, Issue 1, pp.17-21, March 2007.
- C. Yang, F. Liu, T. Ren, L. Liu, H. Feng, Albert Wang and H. Long, "Fully Integrated Ferrite-Based Inductors for RF ICs", *Sensors & Actuators: A. Physical*, A 130-131, p365-370, 2006.
- F. Liu, T. Ren, C. Yang, L. Liu, Albert Wang, and J. Yu, "NiCuZn Ferrite Thin Films for RF Integrated Inductors," *Materials Letter*, Vol. 60, pp. 1403-1406, 2006.
- T. Ren, C. Yang, F. Liu, L. Liu, Albert Z. Wang and X. Zhang, "Equivalent Circuit Analysis of an RF Integrated Inductor with Ferrite Thin-Film," *Journal of Semiconductors*, Vol. 27, pp. 511-515, 2006.
- C. Yang, F. Liu, T. Ren, L. Liu, H. Feng, Z. Albert Wang, H. Long and J. Yu, "RF Integrated Inductor with CoZrO Ferrite Thin Film," *Journal of Semiconductors*, Vol. 26, pp. 2208-2212, 2005.
- Albert Wang, H. Feng, R. Zhan, H. Xie, G. Chen, Q. Wu, X. Guan, Z. Wang and C. Zhang, "A Review on RF ESD Protection Design", *IEEE Trans. Electron Devices*, Vol. 52, No. 7, pp. 1304-1311, July 2005.
- H. Long, Z. Feng, H. Feng, Albert Wang, Tianling, Ren, Junbo Bao, Feng Liu, Chen Yang, Xiao Zhang, "A New Modeling Technique for Simulating 3D

Arbitrary Conductor-Magnet Structures for RFIC Applications”, *IEEE Trans. Electron Devices*, Vol. 52, No. 7, pp. 1354-1363, July 2005.

- H. Xie, H. Feng, R. Zhan, Albert Wang, D. Rodriguez and D. Rice, “A New Low-Parasitic Polysilicon SCR ESD Protection Structure for RF ICs”, *IEEE Electron Device Letters*, Vol. 26, No.2, pp.121-123, February 2005.
- R. Zhan, H. Feng, Q. Wu, H. Xie, X. Guan, G. Chen and Albert Z. Wang, “ESDInspector: A New Layout-level ESD Protection Circuitry Design Verification Tool Using A Smart-Parametric Checking Mechanism”, *IEEE Trans. CAD of Integrated Circuits and Systems*, Vol. 23, No. 10, pp.1421-1428, October 2004.
- G. Chen, H. Feng, H. Xie, R. Zhan, Q. Wu, X. Guan, Albert Wang, K. Takasuka, S. Tamura, Z. Wang and C. Zhang, “Characterizing Diodes For RF ESD Protection”, *IEEE Electron Device Letters*, Vol. 25, No. 5, pp.323-325, May 2004.
- H. Feng, R. Zhan, G. Chen, Q. Wu and Albert Z. Wang, “Electrostatic Discharge Protection for RF Integrated Circuits: New ESD Design Challenges”, *Analog Integrated Circuits and Signal Processing, An International Journal*, Vol. 39, Issue 1, pp. 5-19, April 2004.
- R. Zhan, H. Feng, Q. Wu and Albert Wang, “ESDExtractor: A New Technology-Independent CAD Tool For Arbitrary ESD Protection Device Extraction,” *IEEE Trans. CAD of Integrated Circuits and Systems*, Vol. 22, No. 10, pp.1362-1370, October 2003.
- H. Long, Z. Feng, H. Feng and Albert Wang, “A Novel Accurate PEEC-based 3D Modeling Technique for RF Devices of Arbitrary Conductor-Magnet Structure,” *Microwave and Optical Technology Letters*, V38, Issue 3, Wiley & Sons, pp.237-240, August 2003.
- H. Feng, G. Chen, R. Zhan, Q. Wu, X. Guan, H. Xie, Albert Wang and R. Gafiteanu, “A Mixed-Mode ESD Protection Circuit Simulation-Design Methodology,” *IEEE J. Solid-State Circuits*, V38, N6, pp.995-1006, June 2003.
- H. Feng, R. Zhan, Q. Wu, G. Chen and Albert Wang, “RC-SCR: A Very-Low-Voltage ESD Protection Circuit in Plain CMOS,” *IEE Electronics Letters*, V38, N19, pp.1099-1100, September 2002.
- H. G. Feng, R. Y. Zhan, Q. Wu, G. Chen and Albert Z. Wang, “A Circular Under-Pad Multiple-Mode ESD Protection Structure for ICs,” *IEE Electronics Letters*, V38, N11, pp. 511 –513, May 2002.
- H. G. Feng, K. Gong, R. Zhan and Albert Wang, “A Novel all-Direction on-Chip Protection Circuit,” *IEICE Trans. Electron.*, Vol. E85-C, N3, pp.566-571, March 2002.
- K. Gong, H. Feng, R. Zhan and Albert Z. Wang, “A Study of Parasitic Effects of ESD Protection on RF ICs,” *IEEE Trans. Microwave Theory and Techniques*, V50, N1, pp.393-402, January 2002.
- H. Feng, R. Zhan, K. Gong and Albert Z. Wang, “A New Pad-Oriented Multiple-Mode ESD Protection Structure and Layout Optimization,” *IEEE Electron Device Letters*, V22, N10, pp.493-495, Oct. 2001.

- K. Gong, H. G. Feng, R. Y. Zhan and Albert Z. Wang, "ESD-Induced Circuit Performance Degradation in RFICs," *Microelectronics Reliability*, V41, Issue 9-10, PERGAMON, Elsevier Science, pp.1379-1383, September-October 2001.
- Albert Z. Wang, H. G. Feng, K. Gong, R. Y. Zhan and J. Stine, "On-Chip ESD Protection Design for Integrated Circuits: an Overview for IC Designers," *Microelectronics Journal*, Elsevier Science, V32, Issue 9, pp.733-747, September 2001.
- H. G. Feng, K. Gong, R. Zhan and Albert Wang, "A Pad-Oriented Novel Electrostatic Discharge Protection Structure For Mixed-Signal ICs," in *Advances in Systems Science: Measurement, Circuits and Control*, Edited by N. Mastorakis and L. Pecorelli-Peres, Electrical and Computer Engineering Series, WSES Press, 2001, pp.159-163.
- H. G. Feng, K. Gong, and Albert Z. Wang, "A Novel on-Chip Electrostatic Discharge Protection Design for RFIC's," *Microelectronics Journal*, V32, Issue 3, Elsevier Science, pp 189-195, March 2001.
- Albert Wang and C. Tsay, "On a Dual-Direction on-Chip Electrostatic Discharge Protection Structure," *IEEE Trans. Electron Devices*, V48, N5, pp.978-984, May 2001.
- Albert Wang and C. Tsay, "An on-Chip ESD Protection Circuit with Low Trigger-Voltage in BiCMOS Technology," *IEEE J. Solid-State Circuits*, V36, N1, pp.40-45, January 2001.
- Albert Wang, C. Tsay, and P. Deane, "A Study of NMOS Behaviors under ESD Stress: Simulation and Characterization," *Microelectronics Reliability*, V38, Issue 6-8, PERGAMON, Elsevier Science, pp.1183-1186, 1998.
- Albert Wang & W. Anderson, "Fabrication and Characterization of a Depletion-mode  $Zn_{0.07}Sse_{0.93}$  MESFET," *IEEE Electron Device Lett.*, Vol.17, N5, pp.217-219, May 1996.
- Albert Wang & W. Anderson, "Metal-Semiconductor Contacts to n- $Zn_{0.07}Sse_{0.93}$ ," *J. Electronic Materials*, V25, N2, pp.201-206, February 1996.
- Albert Z. Wang & W. A. Anderson, "Enhancement of the Schottky Barrier Height of Au/ZnSSe Diodes," *Applied Physics Letters*, V66, N15, pp.1963-1965, April 1995.
- Albert Z. Wang, W. A. Anderson, and M. A. Haase, "Electrical Properties of Schottky Contacts to N-type  $Zn_{0.07}Sse_{0.93}$  Epilayers," *J. Applied Physics*, V77, N7, pp.3513-3517, April 1995.
- Albert Z. Wang and W. A. Anderson, "Influence of a Single InGaAs Quantum Well on Current Transport and Deep Levels in GaAs," *Solid State Electronics*, V38, N3, pp.673-678, March 1995.
- Z. H. Wang and X. L. Chen, "On Asymmetric LDD MOSFETs," *J. Semiconductors*, V11, N2, pp.136-141, February 1990.

**Conference Papers:**

- C. Yang, F. Liu, T. Ren, I. Liu, J. Zhan and Albert Wang, "Soft-Ferrite-Film Integration for on-Chip RF Passive Elements", to appear, *International Conference on Communication Technology and VLSI Design (CommV 09)*, Oct., 2009.
- L. Lin, X. Wang, H. Tang, Q. Fang, H. Zhao, Albert Wang, R. Zhan, H. Xie, C. Gill, B. Zhao, Y. Zhou, G. Zhang and X. Wang, "Whole-Chip ESD Protection Design Verification by CAD", **Invited**, *IEEE Proc. EOS/ESD Symp*, pp.28-37, Anaheim, CA, 2009.
- X. Wang, B. Qin, H. Xie, L. Lin, H. Tang, Q. Fang, H. Zhao, S. Wang, Albert Wang, H. Chen, B. Zhao, Y. Zhou, L. Yang and G. Zhang, "FCC-EIRP-Aware UWB Pulse Generator Design Approach", **Invited**, *Proc. IEEE Intl. Conf. Ultra Wideband (ICUWB)*, pp.592-596, Vancouver, Canada, 2009.
- F. Zhang, Z. Wang, X. Wang, H. Tang, Q. Fang, Albert Wang, W. Chen, L. Yang, B. Zhao, G. Zhang, and X. Wang, "Design Optimization and Modeling of on-Chip RF Inductors in 0.13 $\mu$ m and 90nm Standard CMOS", *Proc. IEEE MWSCAS*, pp.975-978, Cancun, Mexico, 2009.
- C. Yang, T. Ren, I. Liu, J. Zhan, X. Wang, Albert Wang, Z. Wu and X. Li, "on-Chip Soft-Ferrite-Integrated Inductors for RF IC", *Proc. IEEE Transducers*, pp. 785-788, Denver, June 2009.
- X. Wang, H. Tang, L. Lin, Q. Fang, H. Zhao, Albert Wang, G. Zhang, X. Wang, Y. Zhou, Lee Yang and H. Chen, "ESD Protection for RF/AMS ICs: Design and Optimization", **Invited**, *Proc. IEEE Intl. Conf. IC Design and Technology (ICICDT)*, pp25-28, Austin, May 2009.
- B. Qin, X. Wang, H. Chen, Albert Wang, Y. Hao, L. Yang and B. Zhao, "A Single-Chip 33pJ/pulse 5<sup>th</sup>-Derivative Gaussian Based IR-UWB Transmitter in 0.13 $\mu$ m CMOS", *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp.401-404, Taipei, May 2009.
- B. Qin, X. Wang, H. Chen, Albert Wang and B. Zhao, "A Programmable 1.8pJ/b Gaussian Pulse Generator for Impulse UWB Transceivers in 90nm CMOS", *Proc. IEEE Radio and Wireless Symposium (RWS)*, pp.498-501, San Diego, 2009. **(Best Student Paper candidate)**
- C. Yang, T. Ren, L. Liu, Y. Yuan, Albert Wang, and X. Wang, "Ferrite-integrated on-chip RF solenoid inductor," 7th IEEE Conference on Sensors (SENSORS), Lecce, Italy, pp. 1040-1043, Oct. 2008.
- Y. Yuan, C. Yang, T. Ren, J. Zhan, L. Liu and Albert Wang, "Design and Simulation of on-Chip Magnetic Inductors for RF ICs," *Proc. IEEE ICSICT, IEEE 978-1-4244-2186-2/08*, pp. 523-526, 2008.
- B. Qin, X. Wang, H. Chen, Albert Wang and B. Zhao, "A Tunable 2.4pJ/b 1<sup>st</sup>-Order Derivative Gaussian Pulse Generator for Impulse UWB Transceivers in 0.13 $\mu$ m CMOS," *Proc. IEEE ICSICT*, pp1544-1547, 2008.
- L. Zhang, R. Huang, Albert Wang, D. Wu, R. Wang, Y. Kuang, "The Parasitic Effects Induced by the Contact in RRAM with MIM Structure", *Proc. IEEE ICSICT*, pp932-935, 2008.
- X. Guan, X. Wang, L. Lin, G. Chen, Albert Wang, H. Liu, Y. Zhou, H. Chen, L. Yang and B. Zhao, "ESD-RFIC Co-Design Methodology", **Invited**, *Proc. IEEE RFIC*, pp467-470, Atlanta, 2008.



- X. Wang, L. Lin, X. Guan, G. Chen, Albert Wang, H. Liu, Y. Zhou, L. Yang, H. Chen and B. Zhao, "ESD-Sensitive LNA Design", *IEEE Proc. Asia-Pacific Symposium on Electromagnetic Compatibility (AP-EMC) and 19<sup>th</sup> International Zurich Symposium on Electromagnetic Compatibility*, pp. 156-159, 2008.
- L. Lin, J. Liu, X. Wang, Albert Wang, H. Liu and Y. Zhou, "3D Electro-Thermal Modeling for ESD protection structures in Sub-100nm CMOS", **Invited**, *Proc. IEEE International Nanoelectronics Conference (INEC)*, pp871-874, 2008.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang, and Z. Yue, "Ferrite-Partially-Filled on-Chip RF Inductor Fabricated Using Low-Temperature Nano-Powder-Mixed-Photoresist Filling Technique for Standard CMOS", *IEEE International Electron Device Meeting (IEDM) Tech. Digest*, pp1038-1040, 2007.
- H. Xie, X. Wang, Albert Wang, B. Zhao, Y. Zhou, B. Qin, H. Chen and Z. Wang, "A Varying Pulse Width 5<sup>th</sup>-Derivative Gaussian Pulse Generator for UWB Transceivers in CMOS", *Proc. IEEE Radio and Wireless Symposium (RWS)*, pp171-174, 2008.
- X. Wang, H. Xie, Albert Wang, B. Qin, H. Chen, S. Qiao, Y. He and Y. Zhou, "Simulation Design of A New 3.1-10.6GHz Single-Full-Band Non-Carrier Pulse-Based Ultra Wideband System", *Proc. IEEE ASICON*, pp834-837, October 2007.
- X. Guan, G. Chen, L. Lin, X. Wang, Albert Wang, L. Yang and B. Zhao, "A New ESD-Aware Power Amplifier Design Method", **Invited**, *Proc. IEEE ASICON*, pp1363-1366, October 2007.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang and H. Feng, "Magnetic film inductors for RF IC", **Invited**, *Proc. ECS Int'l Semiconductor Technology Conference (ECS-ISTC)*, pp447-462, 2007. 2<sup>nd</sup> Place, **Best Student Paper Award**.
- H. Xie, X. Wang, Albert Wang, B. Qin, H. Chen, B. Zhao and L. Yang, "A Broadband CMOS Multiplier-Based Correlator for IR-UWB Transceiver SoC", *Proc. IEEE RFIC*, pp493-496, 2007.
- H. Xie, X. Wang, Albert Wang, B. Qin, H. Chen, Y. Zhou and B. Zhao, "A Varying Pulse Width Second Order Derivative Gaussian Pulse Generator for UWB Transceivers in CMOS", *Proc. IEEE Int'l Symp. Circuits and Systems (ISCAS)*, pp2794-2797, 2007.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan, Albert Wang and Z. Yue, "Ni-Zn Ferrite Film Coated on-Chip RF Inductor Fabricated by A Novel Powder-Mixed-Photoresist Spin-Coating Technique", *Proc. IEEE MTT-S Int'l Microwave Symposium (IMS)*, pp465-468, 2007.
- C. Yang, F. Liu, T. Ren, L. Liu, G. Chen, X. Guan and Albert Wang, "Magnetic film inductors for RF IC", **Invited**, *Proc. ECS Int'l Semiconductor Technology Conference (ECS-ISTC)*, pp447-462, 2007. (Best Student Paper Award 2<sup>nd</sup> Place)
- H. Xie, X. Wang, Albert Wang, Z. Wang and C. Zhang, "A Fully-Integrated Low-Power 3.1-10.6GHz UWB LNA in 0.18 $\mu$ m CMOS", *Proc. IEEE Radio and*

*Wireless Symposium (RWS)*, pp.197-200, January 2007. (Candidate for Best Student Paper)

- C. Yang, F. Liu, T. Ren, L. Liu and Albert Z. Wang, "On-Chip Integrated Inductors with Ferrite Thin-Films for RFIC", *Tech. Digest, IEEE International Electron Devices Meeting (IEDM)*, pp225-228, 2006.
- H. Xie, X. Wang, Albert Wang, B. Qin, H. Chen and B. Zhao, "An Ultra Low-Power Low-Cost Gaussian Impulse Generator for UWB Applications", *Proc. IEEE Int'l Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1817-1820, 2006.
- H. Xie, S. Fan, X. Wang, Albert Wang, Z. Wang and H. Chen, "A Pulse-Based Non-Carrier 7.5GHz UWB Transceiver SoC with on-Chip ADC", **Invited**, *Proc. IEEE Int'l Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1804-1807, 2006.
- C. Yang, F. Liu, T. Ren, L. Liu and Albert Z. Wang, "On-Chip Integrated Inductors with Ni-Zn-Cu-Fe and Y-Bi-Fe Thin-Films for RF IC", *Proc. 34<sup>th</sup> IEEE European Solid-State Device Research Conf (ESSDERC)*, pp. 194-197, September 2006.
- H. Xie, S. Fan, X. Wang, Albert Wang, Z. Wang and H. Chen, "A Pulse-Based Full-Band UWB Transceiver SoC in 0.18 $\mu$ m SiGe BiCMOS", *Proc. IEEE International SoC Conference*, pp.73-76, 2006.
- Albert Wang, "UWB Radio: Big for Wireless Applications", **Invited**, *Proc. CAS IC Design and Application Workshop*, pp. 26-30, 2006.
- Q. Wu, S Fan, Albert Wang, K. Takasuka and S. Takeuchi, "An Optimized Pipelined-Subranging ADC Architecture", *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, paper#: 3249, pp.62, 2006.
- H. Xie, S. Fan, X. Wang and Albert Wang, "An Ultra-Low Power Pulse-Based UWB Transceiver SoC", *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, paper#: 3248, pp.111, 2006.
- X. Guan, H. Feng, Albert Wang, A. Ishikawa, S. Tamura, K. Takasuka, Z. Wang and C. Zhang "A 3V 110uW 3.1ppm/ $^{\circ}$ C Curvature-Compensated CMOS Bandgap Reference", *Proc. IEEE Int'l Symp. on Circuits and Systems (ISCAS)*, pp.2861-2864, 2006.
- X. Guan, H. Feng, Albert Wang and L. Yang, "A New Circuit Model for Designing Fully Integrated Class-A Power Amplifier", *Proc. 25<sup>th</sup> IEEE Int'l Conference on Microelectronics (MIEL)*, **Keynote**, pp. 409-412, 2006.
- Albert Wang, H. Feng, R. Zhan, H. Xie, G. Chen and X. Guan, "RF ESD Protection for VDSM Si Technology", **Invited**, *Proc. ECS 5<sup>th</sup> Int'l Semiconductor Technology Conference (ECS-ISTC)*, 2006.
- H. Xie, L. Lin, Albert Wang and R. Zhan, "Accurate 3D Electro-Thermal Modeling for ESD Protection Structures to Nano Scale", *Proc. International Workshop on Nano CMOS*, **Invited**, pp.68-71, Japan, 2006.
- H. Xie and Albert Wang, "A Fine-Tuned Low-Power LNA for Lower-Band UWB Transceiver", *Proc. IEEE International Conference on Electron Devices and Solid-State Circuits*, **Invited**, pp.217-220, 2005.
- Albert Wang, X. Guan, H. Feng, Q. Wu, R. Zhan and L. Yang, "A 2.4 GHz Fully Integrated Class-A Power Amplifier In 0.35 $\mu$ m SiGe BiCMOS

Technology”, **Invited**, *Proc. IEEE Int’l Conf. on ASIC (ASICON)*, pp.360-363, 2005.

- H. Xie, X. Wang and Albert Wang, “A Fully-Integrated Fine-Tuned Low-Power 3.1-10.6GHz UWB LNA in 0.18 $\mu$ m SiGe BiCMOS”, *Proc. IEEE 35<sup>th</sup> European Microwave Conference*, V3, pp. 1718–1722, 2005.
- G. Chen, H. Feng, Albert Wang and Y. Cheng, “Noise Analysis of ESD Structures and Impacts on a Fully-Integrated 5.5GHz LNA in 0.18 $\mu$ m SiGe BiCMOS”, *Proc. IEEE 35<sup>th</sup> European Microwave Conference*, October 2005.
- Albert Wang, H. Feng, Q. Wu, X. Guan and R. Zhan , “A 2.45GHz Wide Tuning Range VCO Using MOS Varactor in 0.35 $\mu$ m SiGe BiCMOS Technology”, **Keynote**, *Proc. IEEE International Symp. Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications (MAPE)*, pp.10-13, 2005.
- H. Xie, R. Zhan and Albert Wang, “3D Electro-Thermal Modeling for on-Chip ESD Protection Structures”, **Invited**, *Proc. IEEE International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, pp. 877-880, 2005.
- F. Liu, C. Yang, T. L. Ren, L. T. Liu, H. G. Feng, Albert Z. Wang, H. B. Long and J Yu, “Fully Integrated Ferrite-Based Inductors for RF ICs”, *Proc. IEEE International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, Vol 1, pp.895 - 898, 2005.
- Albert Wang, “Advanced on-Chip ESD Protection Design for Integrated Circuits”, **Invited**, *Proc. IEEE Workshop and IEEE EDS Mini-colloquium on Nanometer CMOS Technology (WIMNACT-7)*, pp.9-75, 2005.
- H. Feng, Q. Wu, X. Guan, R. Zhan, Albert Wang and L. W. Yang, “A 5GHz Dual-Band Sub-Harmonic Direct Down-Conversion Mixer In 0.35 $\mu$ m SiGe BiCMOS”, *Proc. IEEE International Symp. on Circuits and Systems (ISCAS)*, pp.4807-4810, 2005.
- Q. Wu and Albert Wang, “A 12bits/200MHz Resolution/Sampling/Power-Optimized ADC In 0.25 $\mu$ m SiGe BiCMOS”, *Proc. IEEE International Symp. on Circuits and Systems (ISCAS)*, pp.6174-6177, 2005.
- R. Zhan, H. Xie, H. Feng and Albert Wang, “ESDZapper: A New Layout-level Verification Tool for Finding Critical Discharging Path under ESD Stress”, *Proc. IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 79-82, 2005.
- H. Xie, R. Zhan and Albert Wang, “3D Electro-Thermal Modeling of GGNMOS ESD Protection Structure”, *Proc. IEEE Asia-Pacific Conf. on Circuits and Systems (APC-CAS)*, pp.61-64, 2004.
- H. Feng, H. Xie, Albert Wang, Y. Cheng and S. Lloyd, “A Full-Monolithic LNA in 0.18 $\mu$ m SiGe: Performance Variation Due to ESD Protection”, **Invited**, *Proc. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Vol 2, pp.1226 – 1229, 2004.
- H. Xie, R. Zhan, Albert Wang and R. Gafiteanu, “Real 3D Electro-Thermal Simulation and Analysis for ESD Protection Structures”, **Invited**, *Proc. IEEE*

*International Caracas Conference on Devices, Circuits and Systems (ICCDACS)*, pp61-64, 2004.

- H. Feng, Albert Wang and L. Yang, "A New 5.5GHz LNA with Gain Control and Turn-off Control for Dual-Band WLAN Systems", *Proc. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Vol 2, pp.1248 - 1251, 2004.
- H. Xie, R. Zhan, H. Feng, G. Chen, Albert Wang and R. Gafiteanu, "A 3D Mixed-Mode ESD Protection Circuit Simulation-Design Methodology", *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, pp243-246, 2004.
- Albert Wang, "Protecting RF ICs: A New Reliability Challenge", **Keynote**, *Proc. IEEE Asia-Pacific Radio Science Conf.*, pp.38-41, 2004.
- G. Chen and Albert Wang, "Evaluating RF ESD Protection Design: An Overview", **Invited**, *Proc. IEEE 11<sup>th</sup> International Symp. Physical & Failure Analysis of ICs (IPFA)*, pp205-208, 2004.
- Albert Wang, "A Review of RF ESD Protection Design", **Invited Plenary**, *Proc. IEEE Workshop on Microelectronics and Electron Devices*, pp.20-23, 2004.
- G. Chen, H. Feng, H. Xie, R. Zhan, Q. Wu, X. Guan, Albert Wang, K. Takasuka, S. Tamura, Z. Wang and C. Zhang, "RF Characterization of ESD Protection Structures", **Invited**, *Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, pp.379-382, 2004.
- H. Long, Z. Feng, H. Feng, Albert Wang and T. Ren, "L-SIMULATOR: A MAGPEEC-Based new CAD Tool for Simulating Magnetic-Enhanced IC Inductors of 3D Arbitrary Geometry", *Proc. IEEE International Symp. Circuits and Systems (ISCAS)*, Vol 5, pp. V-233/237, 2004.
- R. Zhan, H. Feng, H. Xie and Albert Wang, "ESDInspector: A New Layout-level ESD Protection Circuitry Design Verification Tool Using a Smart-Parametric Checking Mechanism", *Proc. IEEE International Symp. Circuits and Systems (ISCAS)*, Vol 5, pp. V217-220, 2004.
- R. Zhan, H. Feng, Q. Wu, X. Guan, G. Chen, H. Xie and Albert Wang, "Concept and Extraction Method of ESD-Critical Parameters for Function-Based Layout Level ESD Protection Circuit Design Verification", *Proc. IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, pp.710-712, 2004.
- Albert Z. Wang, "Review on ESD Protection for RF & Microwave Devices," **Invited**, *Proc. 11<sup>th</sup> IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications (EDMO)*, pp.170-173, 2003.
- Albert Z. Wang, H. Feng, G. Chen, R. Zhan, H. Xie, Q. Wu and X. Guan, "Key Aspects For ESD Protection Design In ICs: Mixed-Mode Simulation And RF/Mixed-Signal ESD Protection," **Invited**, *IEEE 25<sup>th</sup> Int'l Conf. on ASIC (ASICON)*, pp.1000-1005, 2003.
- H. Feng, R. Zhan, Q. Wu, G. Chen, X. Guan, H. Xie and Albert Z. Wang, "Mixed-Mode ESD Protection Circuit Simulation-Design Methodology," *Proc. IEEE Int'l Symp. Circuits and Systems (ISCAS)*, V1, pp.652-655, 2003.

- H. Feng, R. Zhan, G. Chen, Q. Wu, X. Guan, H. Xie and Albert Wang, "Bonding-Pad-Oriented on-Chip ESD Protection Structures for ICs," *Proc. IEEE Int'l Symp. Circuits and Systems (ISCAS)*, V 4, pp.741-744, 2003.
- G. Chen, H. Feng and Albert Wang, "A Systematic Study of ESD Protection Structures for RF ICs," *Proc. IEEE Symp. RF Integrated Circuits (RFIC)*, pp.347-350, 2003.
- H. Long, Z. Feng, H. Feng and Albert Wang, "magPEEC: Extended PEEC Modeling for 3D Arbitrary Electro-Magnetic Devices with Application for M-Cored Inductors," *Proc. IEEE Symp. RF Integrated Circuits (RFIC)*, pp.251-254, 2003.
- Albert Wang, "Recent Developments in ESD Protection for RF ICs," **Invited**, *Proc. IEEE Asia South Pacific Design Automation Conference (ASP-DAC)*, pp.171-178, 2003.
- R. Zhan, H. Feng, G. Chen, Q. Wu, X. K. Guan and Albert Wang, "A New Technology-independent CAD Tool For ESD Protection Device Extraction – ESDEXTRACTOR," *Proc. IEEE/ACM Int'l Conf. Computer Aided Design (ICCAD)*, pp.510-513, 2002.
- R. Zhan, H. Feng, Q. Wu, G. Chen, X. Guan and Albert Wang, "A New Algorithm for ESD Protection Device Extraction Based on Subgraph Isomorphism," *Proc. IEEE Asia-Pacific Conference on Circuits and Systems (APC-CAS)*, pp.361-366, 2002.
- H. Feng, R. Zhan, Q. Wu, G. Chen, X. Guan and Albert Z. Wang, "RC-SCR: A novel low-voltage ESD Protection Circuit with New Triggering Mechanism," *Proc. IEEE Asia-Pacific Conference on Circuits and Systems (APC-CAS)*, pp.97-100, 2002.
- H. Feng, G. Jelodin, K. Gong, R. Zhan, Q. Wu, C. Chen and Albert Wang, "Super Compact RFIC Inductors in 0.18 $\mu$ m CMOS with Copper Interconnects," *Proc. IEEE Microwave Symposium Digest, 2002, IEEE MTT-S International*, V1, pp. 553 –556, 2002.
- Albert Z. Wang, H. Feng, R. Zhan, G. Chen and Q. Wu, "ESD Protection Design for RF Integrated Circuits: New Challenges," **Invited**, *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, pp.411-418, 2002.
- H. Feng, G. Jelodin, K. Gong, R. Zhan, Q. Wu, C. Chen and Albert Wang, "Super Compact RFIC Inductors in 0.18 $\mu$ m CMOS with Copper Interconnects," *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 443 –446, 2002.
- K. Gong, H. Feng, R. Zhan and Albert Z. Wang, "ESD-Induced Circuit Performance Degradation in RFICs," *IEEE Proc. European Symp. Reliability of Electron Devices Failure Physics & Analysis (ESREF)*, pp.1379-1383, 2001.
- H. G. Feng, K. Gong, R. Zhan and Albert Wang, "A Pad-Oriented Novel Electrostatic Discharge Protection Structure For Mixed-Signal ICs," *Proc. WSES/IEEE Conferences: 5<sup>th</sup> Circuits, Systems, Communications & Computers*, pp.3421-3425, 2001.

- H. G. Feng, K. Gong, R. Zhan and Albert Wang, "On-Chip ESD Protection Design for ICs," **Invited Plenary**, *Proc. WSES/IEEE 5<sup>th</sup> CSCC*, pp.4151-4164, 2001.
- H. G. Feng, K. Gong, R. Zhan and Albert Wang, "A Novel all-Direction on-Chip Protection Circuit," *Proc. IEEE/IEICE Int'l Symp. Signals, Systems, and Electronics (ISSSE)*, pp.118-121, 2001.
- H. G. Feng, K. Gong and Albert Wang, "An ESD Protection Circuit for Mixed-Signal ICs," *Proc. IEEE CICC*, pp.493-496, 2001.
- H. G. Feng, K. Gong and Albert Wang, "ESD Protection in Cu vs. Al: More Robustness & Less Parasitics," poster, *Semicon West*, San Francisco, July 2000.
- Albert Wang, H. Feng and K. Gong, "On-Chip Electrostatic Discharge Protection Design in Copper Interconnects: Better ESD Performance with Less Parasitic Effects," poster, *IEEE 43<sup>rd</sup> Midwest Symp. Circuits and Systems*, August 2000.
- H. G. Feng, K. Gong and Albert Wang, "A New Integrated Metal-Semiconductor Simulation Methodology for on-Chip Electrostatic Discharge Protection Design Optimization", *Proc. IEEE/IFIP World Computer Congress Int'l Conference on Design Automation*, pp.81-85, 2000.
- H. G. Feng, K. Gong and Albert Wang, "A Comparison Study of ESD Protection for RFIC's: Performance vs. Parasitics," *Proc. IEEE RFIC Symp.*, pp.235-238, 2000.
- K. Gong, H. G. Feng and Albert Wang, "On Impacts of ESD Protection Structure on Circuit Performance in Aluminum and Copper Interconnects," *Proc. IEEE 1<sup>st</sup> EIT*, paper 106-3, 2000.
- H. G. Feng, K. Gong and Albert Wang, "A Comparison Study of ESD Protection for RFIC's: Performance vs. Parasitics," *IEEE MTT-S Int'l Microwave Symp. Digest*, pp.143-146, 2000.
- Albert Z. Wang, "A New Design for Complete on-Chip ESD Protection," *Proc. IEEE Custom Integrated Circuits Conference*, pp. 87-90, 2000.
- Albert Z. Wang and C. H. Tsay, "A Compact Square-Cell ESD Structure for BiCMOS ICs," *Proc. IEEE BCTM*, pp. 46-49, 1999.
- Albert Wang, C. Tsay and Q. Shan, "A Novel Dual-Direction IC ESD Protection Device," *Proc. IEEE 7<sup>th</sup> Int'l Symp. Physical and Failure Analysis of Integrated Circuits*, pp.151-155, 1999.
- Albert Wang, C. Tsay, J. Bielawski and L. DeClue, "Design Optimization of a Practical ESD Protection Circuit by CAD: A Case Study," *Proc. IEEE 13<sup>th</sup> UGIM Symp.*, pp. 116-119, 1999.
- Albert Wang and C. Tsay, "A Low-Triggering Circuitry for Dual-Direction ESD Protection," *Proc. IEEE Custom Integrated Circuits Conference*, pp 139-142, 1999.
- Albert Wang and C. Tsay, "A Drop-in PtSi Schottky Module for BiCMOS by TCAD," *Proc. AURORA Conf.*, San Jose, CA, February 1999.
- Albert Wang and C. Tsay, "A Novel Design Methodology Using Simulation for on-chip ESD Protection for Integrated Circuits," *Proc. IEEE Intl. Conf. Solid-State & IC Technology*, pp.509-512, 1998.

- Albert Wang, C. Tsay, A. Lele and P. Deane, "A Study of NMOS Behaviors under ESD Stress: Simulation and Characterization," *Proc. IEEE 9<sup>th</sup> European Symp. Reliability of Electron Devices Failure Physics & Analysis*, pp.151-155, 1998.
- Albert Z. Wang, W. A. Anderson, B. J. Wu, M. Haase, and T. J. Mountziaris, "Zn<sub>0.07</sub>Sse<sub>0.93</sub> Metal-Semiconductor Field Effect Transistor," *Proc. IEEE Cornell Conf. Advanced Concepts in High Speed Semiconductor Devices and Circuits*, 1995.
- Albert Z. Wang and W. A. Anderson, "Metal-Semiconductor Contacts to n-Zn<sub>0.07</sub>Sse<sub>0.93</sub>," *Proc. TMS Electronic Material Conference and IEEE Device Research Conference*, 1995.
- Albert Z. Wang and W. A. Anderson, *Proc. Material Research Society Spring Meeting*, 1995.
- X. Chen and Z. H. Wang, "A asymmetric lightly-doped drain MOS field effect transistor," *Proc., IEEE Intl. Conf. Solid-State & IC Technology*, 1990.

### **U. S. PATENTS:**

1. Albert Z. Wang, "Compact Inductor with Stacked Via Magnetic Cores for Integrated Circuits", *US Patent No. 7,262,680*, August 28, 2007.
2. Albert Z. Wang and R. Zhan, "A parameter checking method for on-chip ESD protection circuit physical design layout verification", *US Patent No. 7,243,317B2*, July 10, 2007.
3. Albert Z. Wang, "Bonding pad-oriented all-mode ESD protection structure", *US Patent No. 6,635,931*, October 21, 2003.
4. Albert Z. Wang, "Single structure all-direction ESD protection for integrated circuits", *US Patent No: 6,512,662*, January 28, 2003.
5. Albert Z. Wang, C. H. Tsay and P. Deane, "Dual-Direction Over-Voltage and Over-Current IC Protection Device and Its Cell Structure", *U. S. Patent No. 6,365,924*, April 2, 2002.
6. Albert Z. Wang, C. H. Tsay and P. Deane, "Method for manufacturing a dual-direction over-voltage and over-current IC protection device and its cell structure", *U. S. Patent 6,258,634*, July 10, 2001.